AIW-356 DQ-E01
User Manual

Applicability Type

AIW PN	MPN	Description
AIW-356 DQ-E01	FM160-EAU-01	5G communication module with M.2 interface for Europe, Australia, and Brazil, USB only for data transmission

Revision History

Version	Date	Description
V1.0.0	2023-10-11	First issue
V1.0.1	2024-01-07	Modify Section 3.1

1 Foreword

1.1 Introduction

The document describes the electrical characteristics, RF performance, dimensions and application environment, etc. of AIW-356 DQ-E01 (hereinafter referred to as AIW-356). With the assistance of the document and other instructions, the developers can quickly understand the hardware functions of AIW-356 DQ-E01 modulesand develop products.

2 Overview

2.1 Introduction

AIW-356 DQ-E01 is a highly integrated 5G wireless communication module which uses M.2 form factor interface. Itsupports 5G NR SUB6/LTE FDD/LTE TDD/WCDMA systems and can be applied to most cellular networks of mobile operators in the world.

2.2 Specifications

2.2.1. RF Characteristic

AIW-356 DQ-E01 operating band and data throughput are shown in Table 2-1 and Table 2-2:

Mode	AIW-356 DQ-E01
WCDMA	Band 1/5/8
FDD-LTE	Band 1/3/5/7/8/20/28/32
TDD-LTE	Band 38/40/41/42/43
SA	n1/3/5/7/8/20/28/38/40/41/75/76/77/78
NSA	n1/3/5/7/8/20/28/38/40/77/78
GNSS	GPS/GLONASS/Galileo/BDS/QZSS

Table 2-1 Operating bands

Mode	AIW-356 DQ-E01
WCDMA	Support 3GPP R9, support DC-HSDPA+ /WCDMA. Support QPSK/16-QAM/64-QAM HSUPA: UL peak rate 5.76Mbps, CAT6 DC-HSDPA: DL peak rate 42Mbps, CAT24 WCDMA: DL peak rate 384Kbps, UL peak rate 384Kbps
LTE	Support 3GPP R16, DL-256QAM, UL-256QAM Max support 5DLCA, 2ULCA DL 4X4 MIMO Peak rate UL: 211Mbps, DL: 1.6Gbps

NSA	LTE Modulation: DL-256QAM, UL-256QAM NR Modulation: DL-256QAM, UL-256QAM LTE support max DL 2X2 MIMO NR support max DL 4X4 MIMO UL peak rate 555Mbps, DL peak rate 3.2Gbps
SA	DL-256QAM UL-256QAM Support max 100MHz bandwidth UL 2X2 MIMO, DL 4X4 MIMO Peak rate UL: 900Mbps, DL: 2.47Gbps LTE Modulation: DL-256QAM, UL-256QAM NR Modulation: DL-256QAM, UL-256QAM

Table 2-2 Modulation characteristic & Data throughput

2.2.2. Product Specification

Mode	AIW-356 DQ-E01
Specification	
CPU	Qualcomm SDX62, 4nm process, ARM Cortex-A7, up to 1.5 GHz
Memory	4Gb LPDDRX4+4Gb NAND Flash
Supported OS	Linux / Android / Windows
Power Level	Class 3 (23.5dBm±1.5dB) for WCDMA bands Class 3 (23dBm±1.5dB) for LTE bands Class 3 (23dBm±1.5dB) for NR Sub6 bands Class 2 (26dBm±1.5dB) for n77/78 bands Class 2 (25.5dBm±1.5dB) for b41/n41 bands
Power Supply	DC 3.135V to 4.4V, Typical 3.8V
Temperature	Normal operating temperature: –30°C to +75°C [1] Extended operating temperature: –40°C to +85°C [2] Storage temperature: –40°C to +85°C
Dimensions	30mm × 52mm × 2.3mm
Weight	About 8.5 g
Interface	
Antenna	WWAN Antenna × 4
	Support 4×4 MIMO
Function Interface	Dual SIM, 3V/1.8V SIM1: USIM SIM2: USIM
	Super Speed USB
	High Speed USB
	W_Disable#

	DPR (Dynamic Power Reduction, reserved)
Interface	
Function Interface	LED
	Antenna tuner interface
	I2S
Software	
Protocol Stack	IPV4/IPV6
Firmware update	USB

Table 2-3 Product Specification

Note:

1. When temperature keeps in the range of –30 to 75°C, module can work normally. Module performance meets the 3GPP specifications.
2. When temperature keeps in the range of –40 to 85°C, module performance may be slightly out of 3GPP specifications.

2.3 Application Framework

The peripheral applications for AIW-356 DQ-E01 module are shown in Figure 2-1:

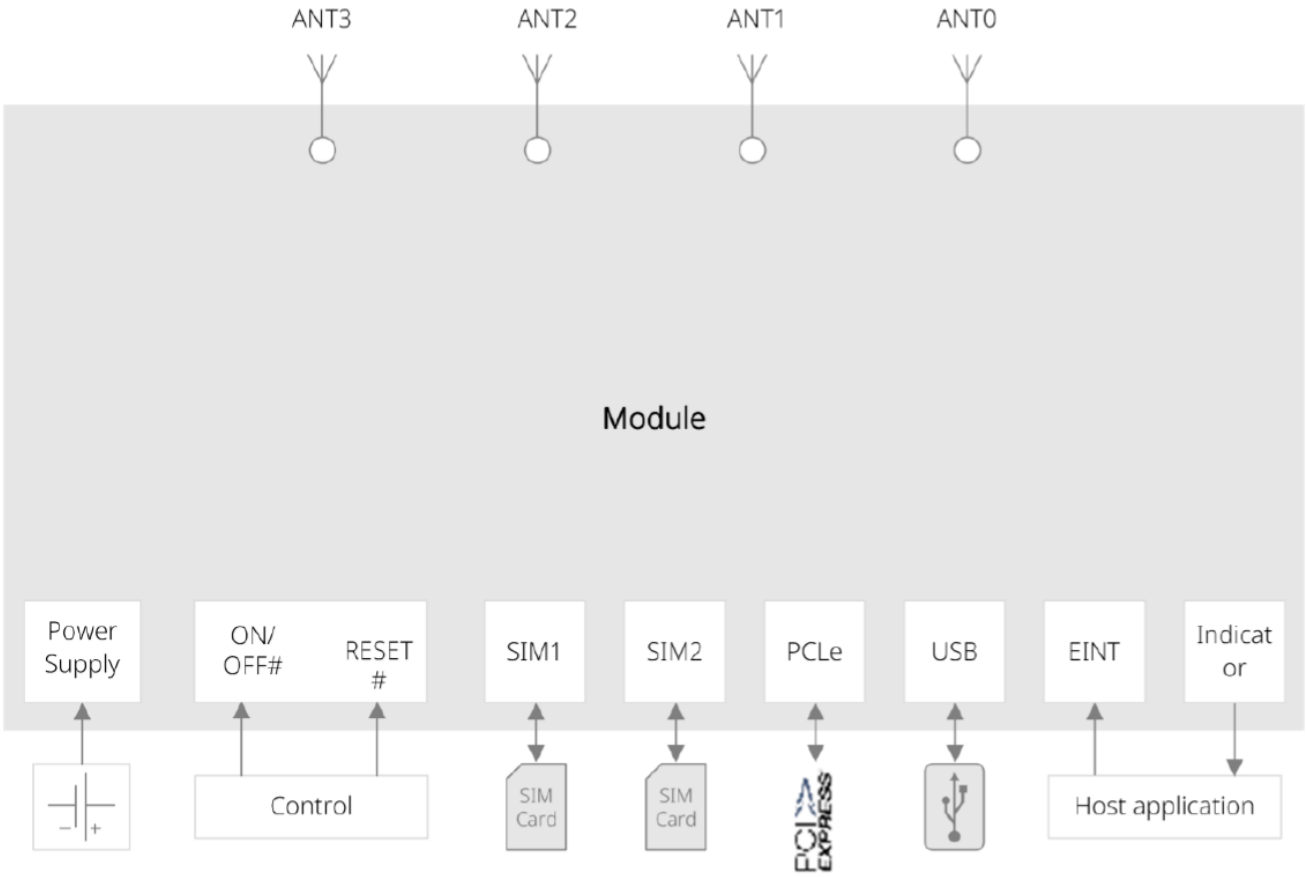


Figure 2-1 Application framework

2.4 Hardware Block Diagram

The hardware block diagram in Figure 2-2 shows the main hardware functions of AIW-356 DQ-E01 module,including baseband and RF functions.

- Baseband functions contain:
  - UMTS/LTE/NR Controller
  - PMU
  - NAND/LPDDR RAM
  - Application Interface
- RF functions contain:
  - RF Transceiver
  - RF Power/PA
  - RF Front End
  - RF Filter
  - Antenna Connector

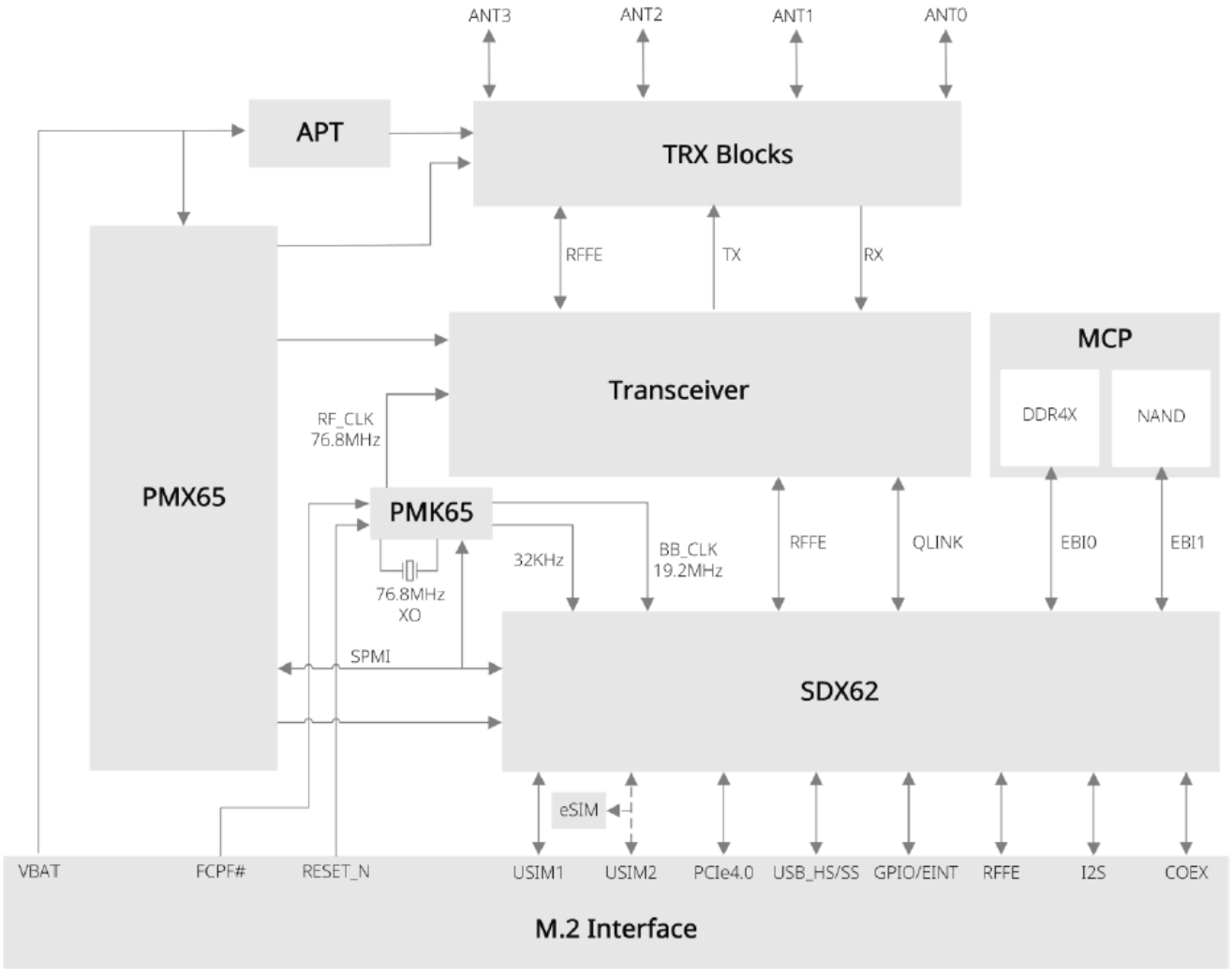


Figure 2-2 Hardware block diagram

2.5 Antenna Configuration

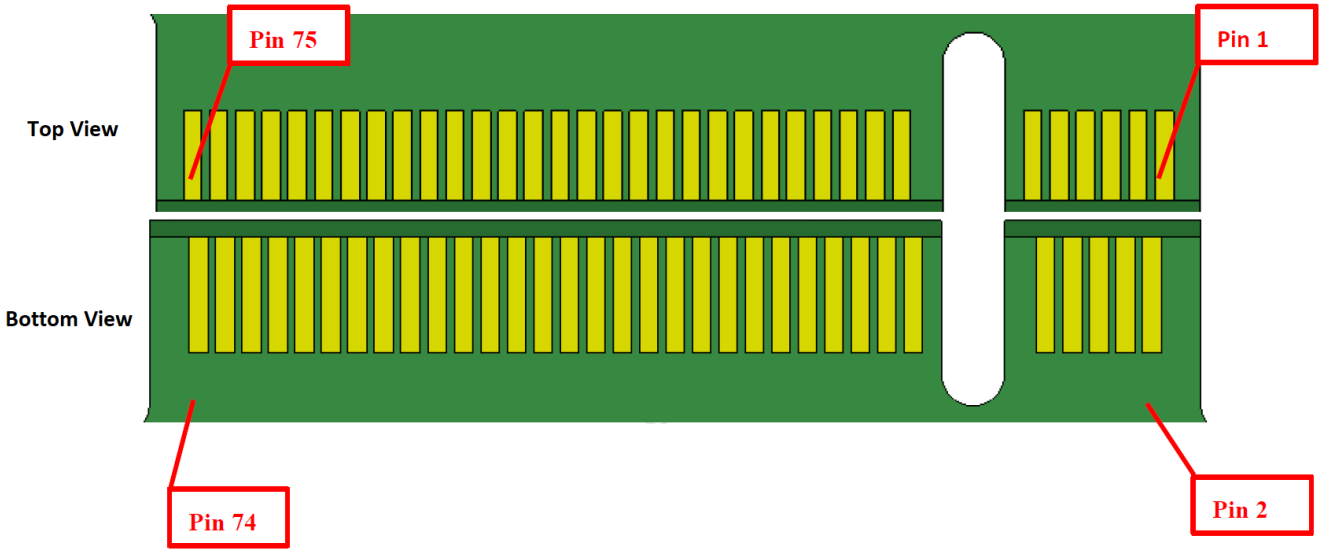
AIW-356 DQ-E01 module supports four antennas and the configuration is shown in the following table:

Pin Name	I/O	Antenna configuration	
ANT0	AIO	Main TX/PRX:	WCDMA: B1 LTE: B1/3/7/38/40/41/42/43 NR: n1/3/7/38/40/41/77/78
		PRX	LTE: B32 NR: n75/76
		Secondary TX / MIMO PRX	LTE: B5/20/28 NR: n5/20/28
ANT1	AIO	Diversity Antenna:	WCDMA: B1/5/8 LTE: B1/3/5/7/8/20/28/32/38/40/41/42/43 NR: n1/3/5/7/8/20/28/38/40/41/75/76/77/78
		GNSS:	L1 RX
ANT2	AIO	MIMO Diversity Antenna:	LTE: B1/3/5/7/20/28/32/38/40/41/42/43 NR: n1/3/5/7/20/28/38/40/41/75/76/77/78
ANT3	AIO	Main TX/PRX:	WCDMA: B5/8 LTE: B5/8/20/28 NR: n5/8/20/28
		MIMO PRX:	LTE: B7/42/43 NR: n7/75/76
		Secondary TX / MIMO PRX	LTE: B1/3/38/40/41 NR: n1/3/38/40/41/77/78

Table 2-5 AIW-356 DQ-E01 module antenna configuration

3 Application Interfaces

3.1. M.2 Key-B Interfaces



3.1.1. Pin Map

Pin No.	AIW-356 DQ-E01		Pin No.
74	VC	CONFIG_2	75
72	VC	NC	73
70	VC	GND	71
68	FORCE_USB_BOOT(1.8V)	CONFIG_1	69
66	SIM Detect (1.8V)	RESET#(3.3V/1.8V)	67
64	COEX1 (1.8V)	ANTCTL3 (1.8V)	65
62	COEX2 (1.8V)	ANTCTL2 (1.8V)	63
60	NC	ANTCTL1 (1.8V)	61
58	RFFE_SDATA(1.8V)	NC	59
56	RFFE_SCLK(1.8V)	GND	57
54	PEWAKE# (3.3/1.8V)	REFCLKP	55
52	CLKREQ# (3.3/1.8V)	REFCLKN	53
50	PERST# (3.3/1.8V)	GND	51
48	UIM2_PWR	PERp0	49
46	UIM2_RESET	PERn0	47
44	UIM2_CLK	GND	45
42	UIM2_DATA	PETp0	43
40	SIM2_DETECT1.8V	PETn0	41
38	NC	GND	39
36	UIM1_PWR	USB_SS-RX+	37
34	UIM1_DATA	USB_SS-RX-	35
32	UIM1_CLK	GND	33
30	UIM1_RESET	USB_SS-TX+	31

Pin No.	AIW-356 DQ-E01		Pin No.
28	I2S_WA (1.8V)	USB_SS-TX-	**29**
26	W_DISABLE2#(3.3/1.8V)	GND	**27**
24	I2S_TX (1.8V)	DPR(3.3/1.8V)	**25**
22	I2S_RX (1.8V)	WOWWAN# (1.8V)	**23**
20	I2S_CLK (1.8V)	CONFIG_0	**21**
	Notch	Notch	
	Notch	Notch	
	Notch	Notch	
	Notch	Notch	
10	LED1#(OD)	GND	**11**
8	W_DISABLE1#(3.3/1.8V)	USB_D-	**9**
6	FULL_CARD_POWER_OFF#	USB_D+	**7**
4	VCC	GND	**5**
2	VCC	GND	**3**
		CONFIG_3	**1**

Figure 3-1 Pin map

Note:

1. The AIW-356 DQ-E01 module applies standard M.2 Key-B interface, with a total of 75 pins.
2. Pin “Notch” represents the gap of the gold fingers. For the location of other pins, refer to Figure 6-1 Structural dimensions.

3.1.2. Pin Definition

Pin	Pin Name	I/O	Reset Value	Description	Type
1	CONFIG_3	O	NC	NC, AIW-356 DQ-E01 M.2 module is configured as the WWAN – PCIe with the USB_SS interface type	-
2	VCC	PI	-	Power input	Power Supply
3	GND	-	-	GND	Power Supply
4	VCC	PI	-	Power input	Power Supply
5	GND	-	-	GND	Power Supply
6	FULL_CARD_ POWER_OFF#	I	PU	Module power-on/off control, the module is powered off when the pin is at low level, and the module is powered on when the pin is floating or at high level. Pulled up through Internal 390KΩ resistor	3.3V/ 1.8V
7	USB D+	I/O	-	USB 2.0 Data+	0.3V-3V
8	W_DISABLE1#	I	PU	Disable flight mode of WWAN module, active low	3.3V/ 1.8V
9	USB D-	I/O	-	USB 2.0 Data–	0.3V-3V
10	LED1#	O	T	System status LED driving pin, OD-gate output.	-
11	GND	-	-	GND	Power Supply
12	Notch	-	-	Notch	-
13	Notch	-	-	Notch	-
14	Notch	-	-	Notch	-
15	Notch	-	-	Notch	-
16	Notch	-	-	Notch	-
17	Notch	-	-	Notch	-

Pin	Pin Name	I/O	Reset Value	Description	Type
18	Notch	-	-	Notch	-
19	Notch			Notch	
20	I2S_CLK	O	PD	I2S Serial clock	1.8V
21	CONFIG_0	-	NC	NC, AIW-356 DQ-E01 M.2 module is configured as the WWAN – PCIe with the USB_SS interface type	-
22	I2S_RX	I	PD	I2S Serial receive data	1.8V
23	WOWWAN#	O	PD	Wake up host	1.8V
24	I2S_TX	O	PD	I2S Serial transmit data	1.8V
25	DPR	I	PU	Dynamic power control for SAR interrupt detection, active low, Reserved	3.3V/ 1.8V
26	W_DISABLE2#	I	PU	Disable GNSS, active low	3.3V/ 1.8V
27	GND	-	-	GND	Power Supply
28	I2S_WA	O	PD	I2S Word selection, left/right channel	1.8V
29	USB_SS -TX-	O	-	Negative end of USB super speed data transmitting	-
30	UIM1_RESET	O	L	SIM1 reset signal	1.8V/ 3V
31	USB_SS -TX+	O	-	Positive end of USB super speed data transmitting	-
32	UIM1_CLK	O	L	SIM card 1 clock	1.8V/ 3V
33	GND	-	-	GND	Power Supply
34	UIM1_DATA	I/O	L	SIM card 1 data	1.8V/ 3V

Pin	Pin Name	I/O	Reset Value	Description	Type
35	USB_SS-RX -	I	-	Negative end of USB super speed data receiving	-
36	UIM1_PWR	PO	-	SIM card 1 power supply, 3V/1.8V	1.8V/ 3V
37	USB_SS-RX+	I	-	USB super speed receive data plus	1.8V
38	NC	-	-	-	-
39	GND	-	-	GND	Power Supply
40	SIM2_DETECT	I	PU	SIM card 2 detection, internally pulled up through 390KΩ resistor, Active high by default	1.8V
41	PETn0	O	-	Negative end of PCIe data TX	-
42	UIM2_DATA	I/O	L	SIM card 2 data	3V/ 1.8V
43	PETp0	O	-	Positive end of PCIe data TX	-
44	UIM2_CLK	O	L	SIM2 clock	3V/ 1.8V
45	GND	-	-	GND	Power Supply
46	UIM2_RESET	O	L	SIM card 2 reset	3V/ 1.8V
47	PERn0	I	-	Negative end of PCIe data RX	-
48	UIM2_PWR	PO	-	SIM card 2 power supply	3V/ 1.8V
49	PERp0	I	-	Positive end of PCIe data RX	-
50	PERST#	I	PU	Module PCIe interface reset. Active low, internally pulled up through 4.7KΩ resistor	3.3V/ 1.8V
51	GND	-	-	GND	Power Supply

Pin	Pin Name	I/O	Reset Value	Description	Type
52	CLKREQ#	I/O	PU	Device requests a PCIe reference clock to transmit data. It is also used by L1 power management status mechanism. Host or device initiates an L1 exit. Active low, An external pull-up resistor must be reserved.	3.3V/ 1.8V
53	REFCLKN	I	-	PCIe Reference Clock signal Differential Negative	-
54	PEWAKE#	O	PU	Wake up system and restore PCIe link from L2 to L0, depending on whether the system supports wakeup functionality. Active low, An external pull-up resistor must be reserved	3.3V/ 1.8V
55	REFCLKP	I	-	PCIe Reference Clock signal Differential Positive	-
56	RFFE_SCLK	O	PD	RFFE-MIPI serial clock signal	1.8V
57	GND	-	-	GND	Power Supply
58	RFFE_SDATA	I/O	PD	RFFE-MIPI serial data signal	1.8V
59	NC	-	-	-	-

Pin	Pin Name	I/O	Reset Value	Description	Type
60	WLAN_TX_EN	I	-	A high level on this pin disables n79 LNAs. Normally this signal is from external 5 GHz WLAN when its transmitting power exceeds a threshold.	-
61	ANTCTL1	O	PD	Tunable antenna control bit 1	1.8V
62	COEX_2	I	PD	BT-SIG based module public network RF and WiFi/BT wireless coexistence management. This function is used specifically for UART receiving.	1.8V
63	ANTCTL2	O	PD	Tunable antenna control bit 2	1.8V
64	COEX_1	O	PD	BT-SIG based module public network RF and WiFi/BT wireless coexistence management. This function is used specifically for UART receiving.	1.8V
65	ANTCTL3	O	PD	Tunable antenna control bit 3	1.8V
66	SIM1_DETECT	I	PU	SIM card 1 Detection, pulled up through 390KΩ internal resistor, Active high by default, indicating SIM card available	1.8V

Pin	Pin Name	I/O	Reset Value	Description	Type
67	RESET#	I	PU	Module reset, pulled up through 390KΩ internal resistor, active low	3.3V/ 1.8V
68	FORCE_USB_BOOT	I	-	After the pin is pulled up to 1.8V during power-on, the module will enter the USB download mode. The pin is used for updating the software of module If it is floating or pulled to low level, the level, the module will enter the normal mode.	1.8V
69	CONFIG_1	O	GND	GND, AIW-356 M.2 module is configured as the WWAN – PCIe with the USB_SS interface type	-
70	VCC	PI	-	Power input	Power Supply
71	GND	-	-	GND	Power Supply
72	VCC	PI	-	Power input	Power Supply
73	NC	-	-	-	-
74	VCC	PI	-	Power input	Power Supply
75	CONFIG_2	O	NC	NC, AIW-356 M.2 module is configured as the WWAN – PCIe with the USB_SS interface type	-

Table 3-1 Pin definition

Reset Value: The initial status after module reset, not the status when working.

H: High Level

L: Low Level

PD: Pull-Down

PU: Pull-Up

T: Tri-state, high resistance

OD: Open Drain

PI: Power Input

PO: Power Output

Note:

1. The unused pins can be left floating.
2. All interfaces that support 3.3V voltage are based on the input voltage of +3.3V power supply. When the input voltage range of the power supply changes from 3.135V to 4.4V, the corresponding interface voltage changes accordingly.

3.2. Power Supply

Pin	Pin Name	I/O	Pin Description	DC Parameter (V)		
				Minimum Value	Typical Value	Maximum Value
2, 4, 70, 72, 74	VCC	PI	Power supply input	3.135	3.8	4.4
36	UIM1_PWR	PO	USIM power supply	-	1.8V/3V	-
48	UIM2_PWR	PO	USIM power supply	-	1.8V/3V	-

Table 3-2 AIW-356 DQ-E01 module power interface

3.2.1. Power Supply

The AIW-356 DQ-E01 module should be powered through the VCC pins, with the continuous current ability greaterthan 2.5A, and the power supply design is shown in Figure 3-2:

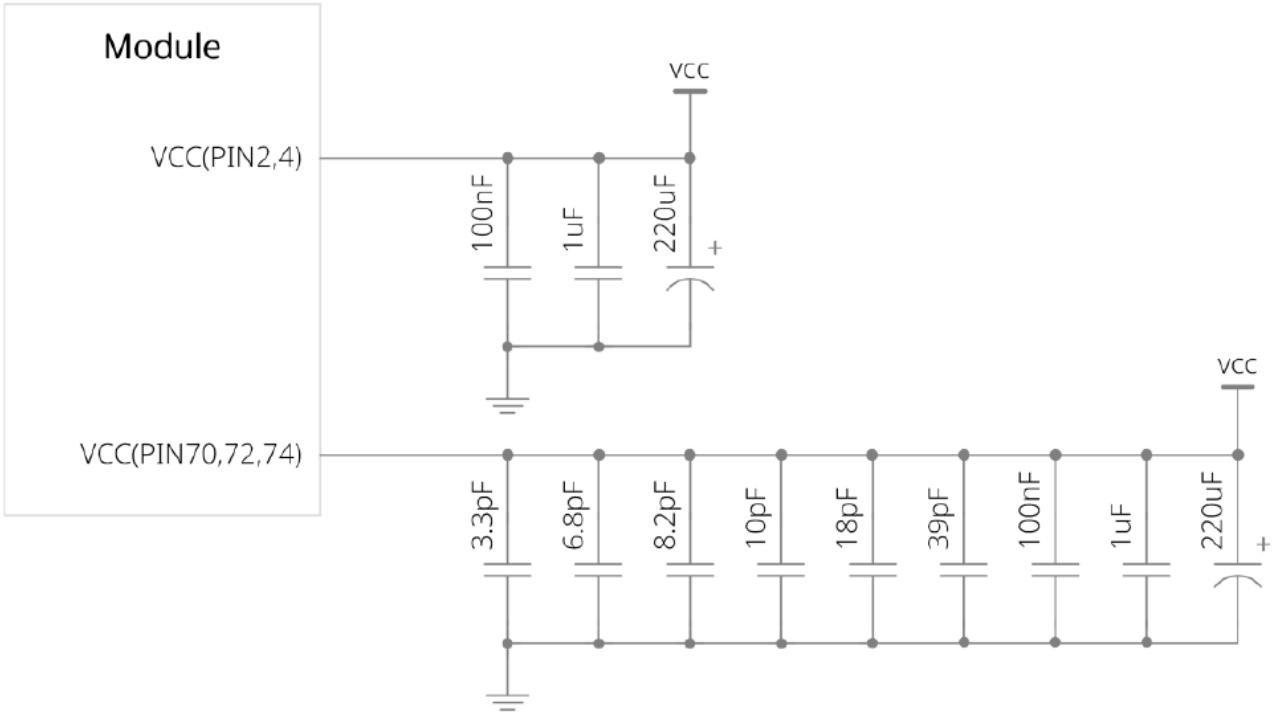


Figure 3-2 Power supply design

Recommended Capacitance	Application	Description
220uF x 2	Voltage regulating capacitors	To reduce power fluctuations of the module inoperation, use low-ESR capacitors. For LDO or DC/DC power supply, the capacitance should be no less than 440uF. For battery power supply, the capacitance can be reduced to 100 uF to 200uF.
1uF, 100nF	Digital signal noise	Filter out the interference generated from the clock and digital signals
39pF, 33pF	700/800 MHz, 850/900MHz frequency band	Filter out low frequency band RF interference
18pF, 10pF, 8.2pF, 6.8pF, 3.3pF	1500/1700/1800/1900MHz, 2100/2300MHz, 2500/2600MHz, 3500/3700MHz, 5GHz frequencyband	Filter out medium/high frequency band RFinterference

Table 3-3 Filter capacitor design for power supply

A stable power supply ensures the normal operation of AIW-356 DQ-E01 module. Make sure that the ripple of the power supply less than 300mV in design. Ensure the power source voltage should be not lower than 3.135V when in MAX consumption mode, otherwise the module may shut down or restart. The power supply requirement is shown in the following Figure 3-3:

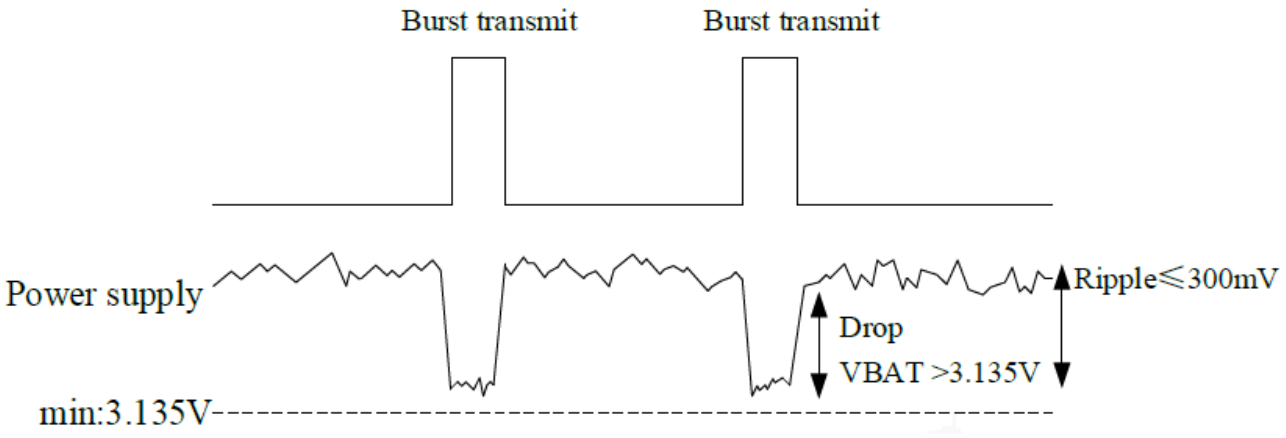


Figure 3-3 Power supply requirement

3.2.1. Logic Level

Parameter	Minimum	Typical	Maximum	Unit
1.8V logic level	1.71	1.8	1.89	V
V_{IH}	1.2	1.8	2.0	V
V_{IL}	-0.3	0	0.3	V

Table 3-4 Definition of 1.8V logic level

Parameter	Minimum	Typical	Maximum	Unit
3.3V logic level	3.135	3.3	3.465	V
V_{IH}	2.3	3.3	3.6	V
V_{IL}	-0.3	0	0.3	V

Table 3-5 Definition of 3.3V logic level

3.2.2. Power Consumption

The following table lists power consumption data of the AIW-356 DQ-N01 module under 3.8V power supply.

State	Mode	Condition	Typical Current/mA
Ioff	Power off	Power supply, module power-off	0.120
I_{IDLE} (USB Disconnection.)	WCDMA	DRX=8	55.1
	LTE FDD	DPC (Default Paging Cycle) =#128	55.9
	LTE TDD	DPC (Default Paging Cycle) =#128	56
	SA	Long DRX (ms10)	53.5
	Radio Off	AT+CFUN=4 Flight Mode	53.4
I_{SLEEP} (USB Disconnection.)	WCDMA	DRX=8	2.3
	LTE FDD	DPC (Default Paging Cycle) =#128	2.9
	LTE TDD	DPC (Default Paging Cycle) =#128	2.6
	SA	Long DRX (ms10)	8
	Radio Off	AT+CFUN=4 Flight Mode	1.7
IWCDMA-RMS	WCDMA	WCDMA Data call Band 1 @+23.5dBm	730
		WCDMA Data call Band 8 @+23.5dBm	635
$I_{LTE-RMS}$	LTE FDD	LTE FDD Data call Band 1 @+23dBm	789.8
		LTE FDD Data call Band 3 @+23dBm	855.8
		LTE FDD Data call Band 5 @+23dBm	594.8
		LTE FDD Data call Band 8 @+23dBm	655.0
	LTE TDD	LTE TDD Data call Band 34 @+23dBm	372
		LTE TDD Data call Band 38 @+23dBm	490.2
		LTE TDD Data call Band 39 @+20dBm	351
		LTE TDD Data call Band 40 @+23dBm	489.2
		LTE TDD Data call Band 41 @+20dBm	680
	LTE HPUE	LTE TDD Data call Band 41 @+25.5dBm	904.3

State	Mode	Condition	Typical Current/mA
$I_{LTE-RMS}$	EN-DC HPUE	EN-DC Data call B1+n78 @23dBm+23dBm	1150
		EN-DC Data call B3+n78 @23dBm+23dBm	1204
		EN-DC Data call B5+n78 @23dBm+23dBm	931
		EN-DC Data call B8+n78 @23dBm+23dBm	1230
		EN-DC Data call B3+n79 @23dBm+23dBm	1245
		EN-DC Data call B39+n79 @23dBm+23dBm	721
		EN-DC Data call B3+n41 @23dBm+23dBm	1260
		EN-DC Data call B39+n41 @23dBm+23dBm	743
I_{SA-RMS}	SA FDD	n1@max power @23dBm (10MHz, Inner full RB)	736.4
		n28@max power @23dBm (10MHz, Inner full RB)	696
	SA TDD	n41@max power @23dBm (100MHz, Inner full RB)	502.2
		n78@max power @23dBm (100MHz, Inner full RB)	452
		n79@max power @23dBm (100MHz, Inner full RB)	423
	SA TDD HPUE	n41@max power @25.5dBm (100MHz, Inner full RB)	615.3
		n78@max power @26dBm (100MHz, Inner full RB)	529.7
		n79@max power @26dBm (100MHz, Inner full RB)	488
	SA UL MIMO	n41@max power @24.5dBm (100MHz, Inner full RB)	648
		n78@max power @24.5dBm (100MHz, Inner full RB)	604
		n79@max power @24.5dBm (100MHz, Inner full RB)	592

Table 3-6 Power consumption of 3.8V power supply

Note:

3.4.1. The data above is an average value of the test results conducted on some samples at 25°Ctemperature.

3.4.2. The LTE power consumption data is a test result conducted on 10MHz 1RB.

3.4.3. The NR power consumption data is a test result conducted on DFT-s-OFDM/QPSK, Inner Full RB.

3.4.4. The NR UL MIMO power consumption data is based on CP-OFDM / QPSK, Inner Full RB.

3.3. Control Signals

The AIW-356 DQ-E01 module provides two control signals for power-on/off and reset operations, the pins are defined in the following table:

Pin	Pin Name	I/O	Reset Value	Description	Type
6	FULL_CARD_POWER_OFF#	I	PU	Module power-on/off control Pulled up through internal 470KΩ resistor Power-on: High/Floating Power-off: Low	3.3V/ 1.8V
67	RESET#	I	PU	Module reset, pulled up through internal 390KΩresistor, active low	3.3V/ 1.8V
50	RESET#	I	PU	Module PCIe interface reset. Active low, Pulled up through internal4.7KΩ resistor	3.3V/ 1.8V

Table 3-4 Module power-on/off and reset

Note:

RESET # and PERST # need to be controlled by independent GPIO which cannot be shared with other devices on the host. RESET # and PERST # are sensitive signals. During PCB layout, keep these signals far away from radio frequency interference. PCB routes must be protected using GND and kept away from edges of PCBs to avoid module reset due to ESD problems.

3.3.1. Module Power-on

3.3.1.1. Power-on Circuit

When the FCPO# (FULL_CARD_POWER_OFF#) pin and reset (RESET#) pin are floating or connect to an external 3.3V/1.8V, the module will boot up. When AP (Application Processor) controls the module start-up, it is recommended that the FULL_CARD_POWER_OFF# and RESET# GPIO port should use a port with low level for reset or internal pull down and the external pull-down resistance should be reserved.The circuit design is shown in Figure 3-4:

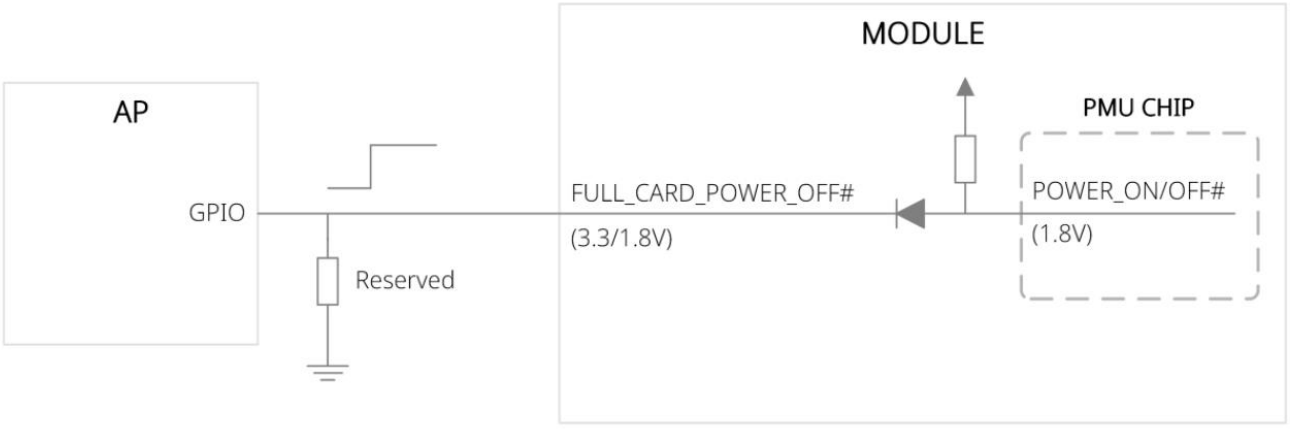


Figure 3-4 Circuit for module start-up controlled by AP

3.3.1.2. Power-on Timing

When power supply is ready, the PMU of module will power on and start initialization process by pullinghigh both FCPO# (Pin6) and RESET# (Pin67) signal. After about 30s, the initialization process of the module will be completed. The power-on timing is shown in Figure 3-5:

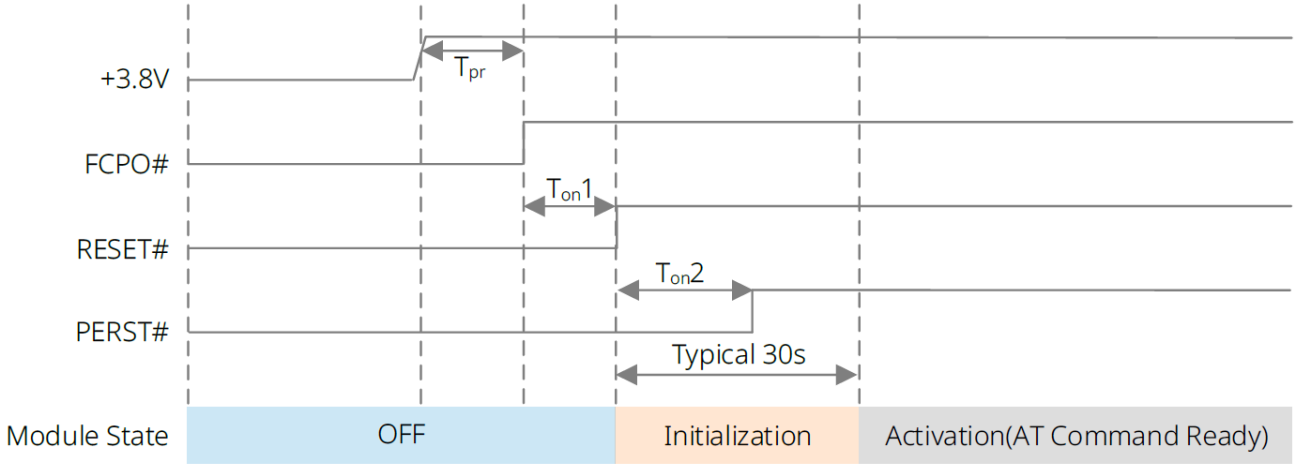


Figure 3-5 Power-on timing

Index	Min.	Recommended	Max.	Remarks
tpr	0ms	-	-	Delay time of FCPO# relative to power ready(3.135V)
ton1	0ms	-	-	Delay time of RESET# signal relative to FCPO# signal
ton2	50ms	100ms	-	Delay time of PERST# signal relative to FCPO# signal, PERST# must always be the last signal to pull up during power-on

Table 3-5 Power-on timing

Note:

1. When only USB interface is used as the data transmission interface, PERST # is left floating. Ignore the control timing in the figure above.

3.3.2. Module Power-off

AIW-356 DK-JK1 module can be powered off by the following control methods, as listed in the table:

Power-off Mode	Action	Condition
Recommend	Send **AT+CPWROFF** command, and then Pull down FCPO# pin	The module normally runs.
Hardware	Pull down FCPO# pin	Used for abnormal status, no response after the **AT+CPWROFF** command is sent

Table 3-6 Module Power off

By sending **AT+CPWROFF** command, the module will start the finalization process (the reverse processof initialization), and it will be completed after tsd time (tsd is the time when the AP receives OK of **AT+CPWROFF** command, if there is no response, max tsd is 5s). In the finalization process, the module will save the network, SIM card and some other parameters from memory, log out, then clear the memoryand shut down PMU. The recommended power-off timing is shown in Figure 3-6:

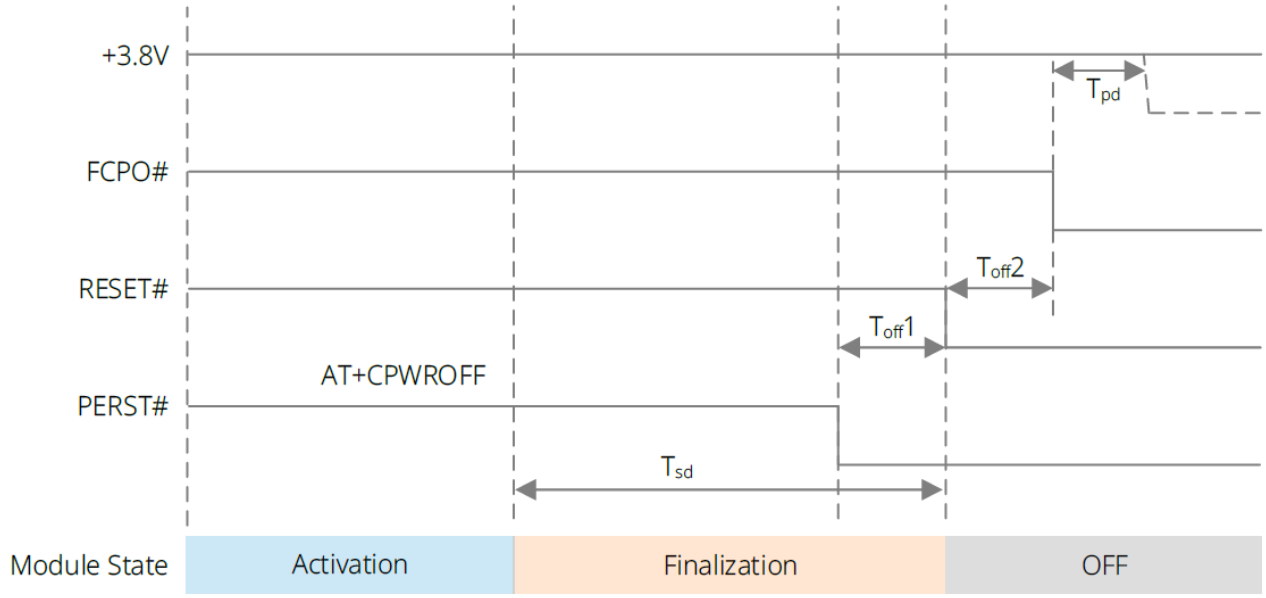


Figure 3-6 Recommended power-off timing

Index	Min.	Recommended	Max.	Comment
t_{off1}	16ms	20ms	-	Pull-down delay time of RESET# signal relative to PERST# signal
ton1	0ms	-	-	Pull-down delay time of FCPO# signal relative to RESET# signal
tpd	10ms	100ms	-	+3.8V power supply off delay time. If power supply is always on +3.8V, it can be ignored

Table 3-7 Power-off timing

Note:

1. When only USB is used as the data transmission interface, keep PERST # floating, and ignore the control timing in the figure above.

3.3.3. Module Reset

The AIW-356 DQ-E01 module can reset to its initial status by pulling down the RESET# signal for more than 30ms(50ms is recommended), and module will restart after RESET# signal is released. The recommended circuit design is shown in the Figure 3-7:

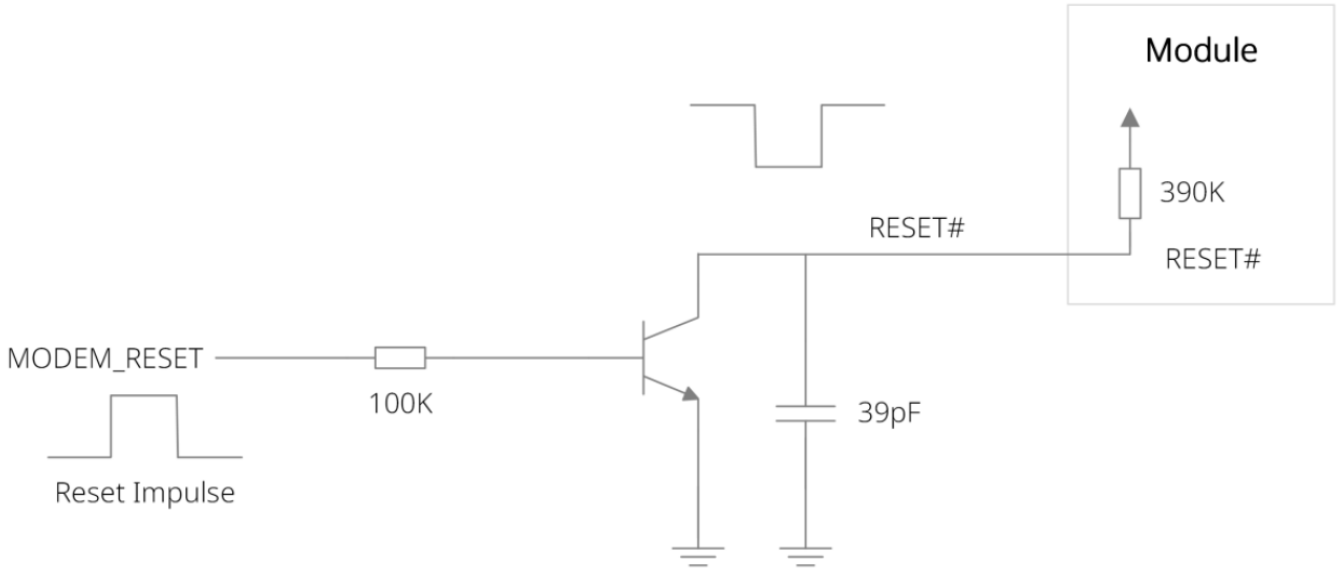


Figure 3-7 Recommended design for reset circuit

There are two reset control timings as below:

- Reset timing 1st in Figure 3-8.
- The Host can only control RESET # when restarting the module, and the module PMU is powered off during reset. It is recommended to use a USB interface connection.
- Reset timing 2nd in Figure 3-9.
- The module PMU is powered off during reset (including complete power-off and power-on timing. For tsd, refer to section 3.2.1.2). It is recommended to use it during hostrestart.

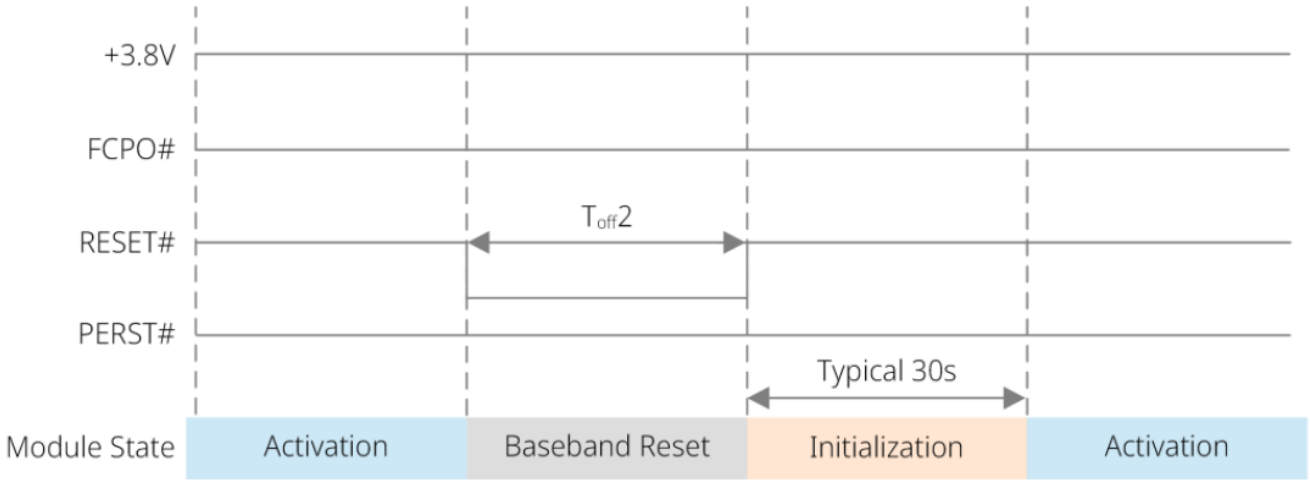


Figure 3-8 Reset timing 1st

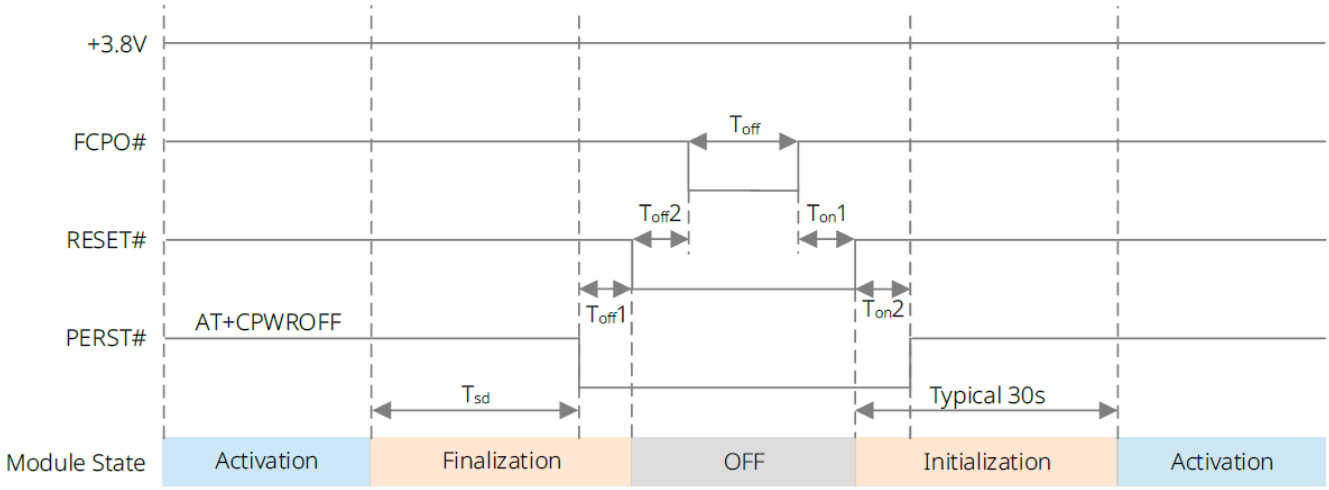


Figure 3-9 Reset timing 2nd

Index	Min.	Recommended	Max.	Remarks
t_{off1}	16ms	20ms	-	Pull-down delay time of RESET# signal relative to PERST#. For details, refer to section 3.3.2
t_{off2}	0	-	-	Pull-down delay time of FCPO# signal relative to RESET#. For details, refer to section 3.3.2
t_{off}	500ms	500ms	-	Power-off time must be not less than 500ms to ensure the module is completely discharged
t_{on1}	0	-	-	Delay time of RESET# signal relative to FCPO#. For details, refer to section 3.3.1.2
t_{on2}	50ms	100ms	-	Delay time of PERST# signal relative to FCPO# signal. PERST# must always be the last signal to pull up during power-on. For details, refer to section 3.3.1.2

Table 3-8 Reset timing

Note:

2. RESET# is a sensitive signal, it's recommended to add a filter capacitor near the module. In case of PCB layout, the RESET# signal lines should be kept away from the RF interference and protected by GND. Also, the RESET# signal lines shall be kept away from the PCB edgeand the surface planes to avoid module reset caused by ESD problems.
3. If the PCIe and USB interfaces are connected to the host, and USB is used as the data transmission interface, the PERST# timing can be ignored.

3.4. USB Interfaces

AIW-356 DQ-E01 module supports USB2.0 and is compatible with USB High-Speed (480 Mbit/s) and USB Full-Speed (12 Mbit/s). At the same time, AIW-356 DQ-E01 also supports USB_3.1 Gen2 10Gbit/s to achieve ultra-high-speed data transmission, which is used to meet the high-speed transmission requirements of 5G mobile networks. For the USB bus timing and electrical specification of AIW-356 DQ-E01 module, please refer toUniversal Serial Bus Specification 2.0 and Universal Serial Bus Specification 3.1.

During AIW-356 DQ-E01 module initialization, the USB can work with the driver to map several ports in Android/Linux system. The ports can be configured according to practical application.

3.4.1. USB Interface Definition

Pin No.	Pin Name	I/O	Description	Type
7	USB D+	I/O	USB 2.0 Data +	0.3V-3V
9	USB D-	I/O	USB 2.0 Data–	0.3V-3V
29	USB_SS_TX-	O	Negative end of USB Super speed data transmitting	-
31	USB_SS _TX+	O	Positive end of USB Super speed data transmitting	-
35	USB_SS _RX-	I	Negative end of USB Super speed data receiving	-
37	USB_SS _RX+	I	Positive end of USB Super speed data receiving	-

Table 3-9 Definition of USB interface

3.4.2. USB2.0 Interface Application

The reference circuit is shown in Figure 3-10:

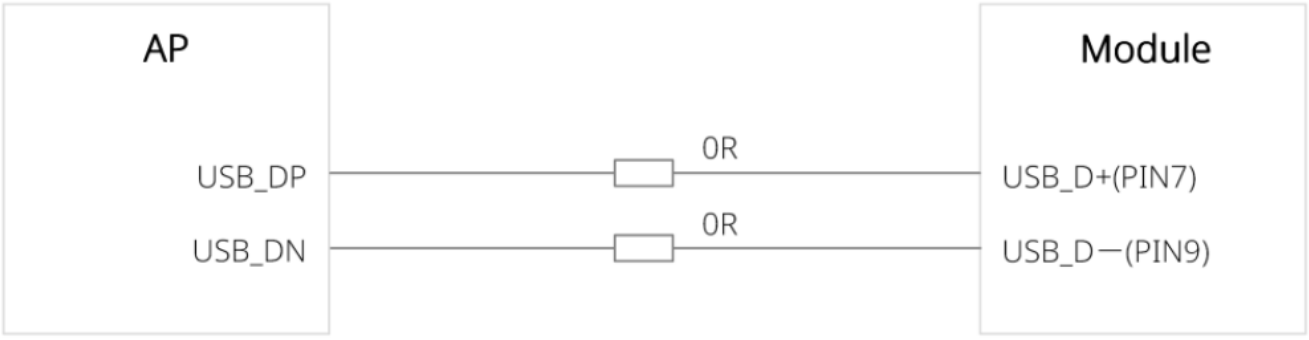


Figure 3-10 Reference circuit for USB 2.0 interface

USB_D- and USB_D+ are high speed differential signal lines with the maximum transfer rate of 480 Mbit/s.The following rules shall be followed carefully in the case of PCB layout:

- USB_D- and USB_D+ signal lines should have the differential impedance of 90±10Ω.
- USB_D- and USB_D+ signal line difference must be less than 2mm in length and parallel, avoidingthe right-angle routing.
- USB_D- and USB_D+ signal lines should be routed on the layer that is closest to the ground layer, and protected with GND vertically and horizontally.

3.4.3. USB3.1 Interface Application

The reference circuit is shown in Figure 3-11:

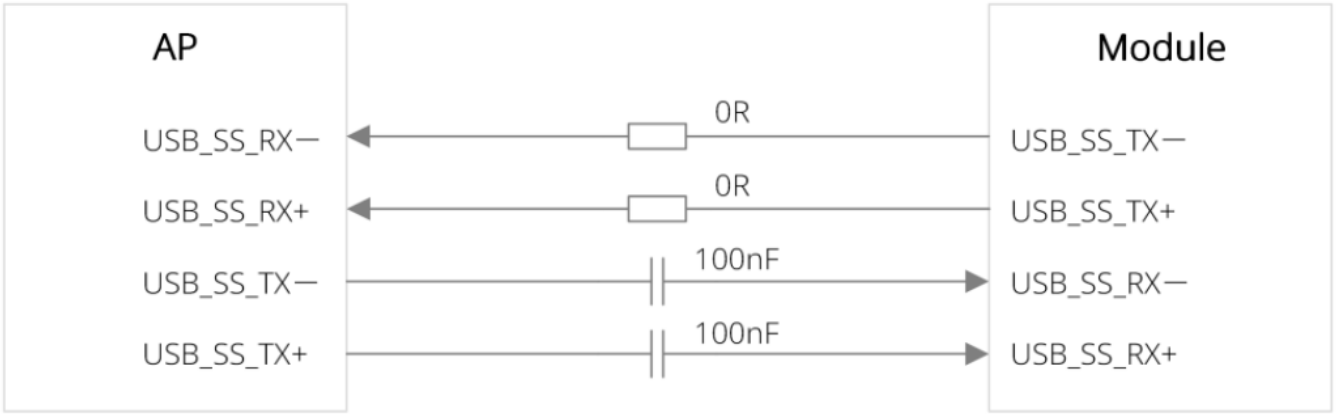


Figure 3-11 Reference circuit for USB 3.1 interface

USB 3.1 Gen2 signals are super speed differential signal lines with the maximum transfer rate of 10Gbps. The following rules shall be followed carefully in the case of PCB layout:

- USB_SS_TX-/USB_SS_TX+ and USB_SS_RX-/ USB_SS_RX+ are two pairs of differential signal lines, and their differential impedance should be controlled as 90±10Ω.
- For TX differential line, the + and – routes must be parallel with equal length, and the length difference should be controlled less than 0.7mm, avoiding right-angle routes.
- For the RX differential line, the + and – routes must be parallel with equal length, and the length difference should be controlled less than 0.7mm., avoiding right-angle routes.
- TX and RX routes must be parallel with equal length, and the length difference should be controlled less than 10mm, avoiding right-angle routes.
- The two pairs differential signal lines should be routed on the layer that is closest to the ground layer, and protected with GND vertically and horizontally.

3.5. USIM Interfaces

The AIW-356 DQ-E01 module supports dual USIM card interfaces and single standby. The SIM card interfacessupport 1.8V and 3V SIM cards.

3.5.1. USIM1 Pins

The USIM1 pins are listed in the following table:

Pin	Pin Name	I/O	Reset Value	Description	Type
36	UIM1_PWR	PO	-	USIM1 power supply	1.8V/3V
30	UIM1_RESET	O	L	USIM1 reset	1.8V/3V
32	UIM1_CLK	O	L	USIM1 clock	1.8V/3V
34	UIM1_DATA	I/O	L	USIM1 data, internally pulled up (20KΩ)	1.8V/3V
66	SIM1_DETECT	I	PU	USIM1 card detection, internally pulled up (390KΩ). Active high by default. And high level indicates a SIM card is inserted; and low level indicates a SIM card is removed.	1.8V

Table 3-10 USIM1 pin definition

3.5.2. USIM2 Pins

The USIM2 pins are listed in the following table:

Pin	Pin Name	I/O	Reset Value	Description	Type
48	UIM2_PWR	PO	-	USIM2 power supply	1.8V/3V
46	UIM2_RESET	O	L	USIM2 reset signal	1.8V/3V
44	UIM2_CLK	O	L	USIM2 clock	1.8V/3V
42	UIM2_DATA	I/O	L	USIM2 data, internally pulled up (20KΩ)	1.8V/3V
40	SIM2_DETECT	I	PU	USIM2 card detection, internally pulled up (390KΩ). Active high by default. And high level indicates a SIM card is inserted; and low level indicates a SIM card is removed.	1.8V

Table 3-11 USIM2 pin definition

3.5.3. USIM Interface Circuit

3.5.3.1. N.C. SIM Card Slot

The reference circuit design for N.C. (Normally Closed) SIM card slot is shown in Figure 3-12:

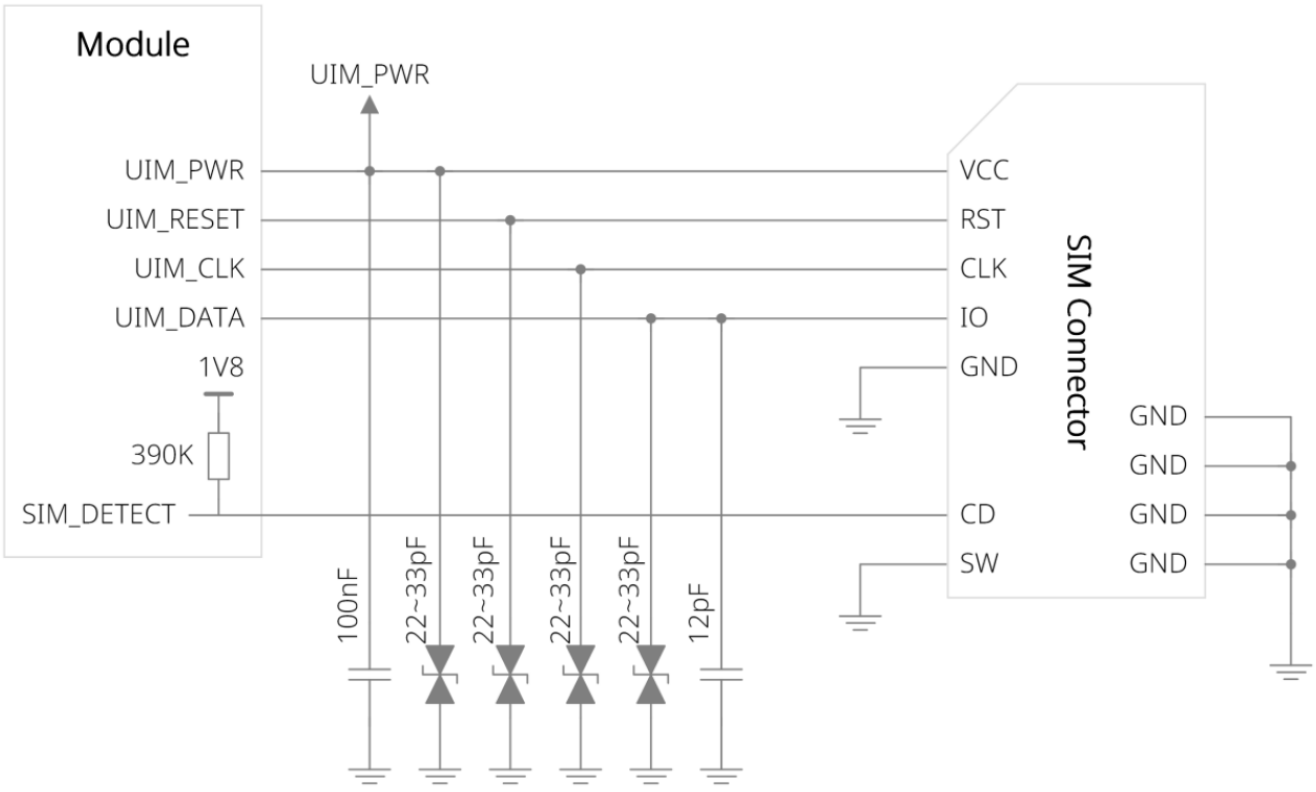


Figure 3-12 Reference circuit for N.C. SIM card slot

The principles of the N.C.SIM card slot are described as follows:

- When the SIM card is removed, CD and SW pins are short-circuited, and the SIM_DETECT pin is at low level.
- When the SIM card is inserted, CD and SW pins are open-circuited, and the SIM_DETECT pin is at high level.

3.5.3.2. N.O. SIM Card Slot

The reference circuit design for N.O. (Normally Open) SIM card slot is shown in Figure 3-13:

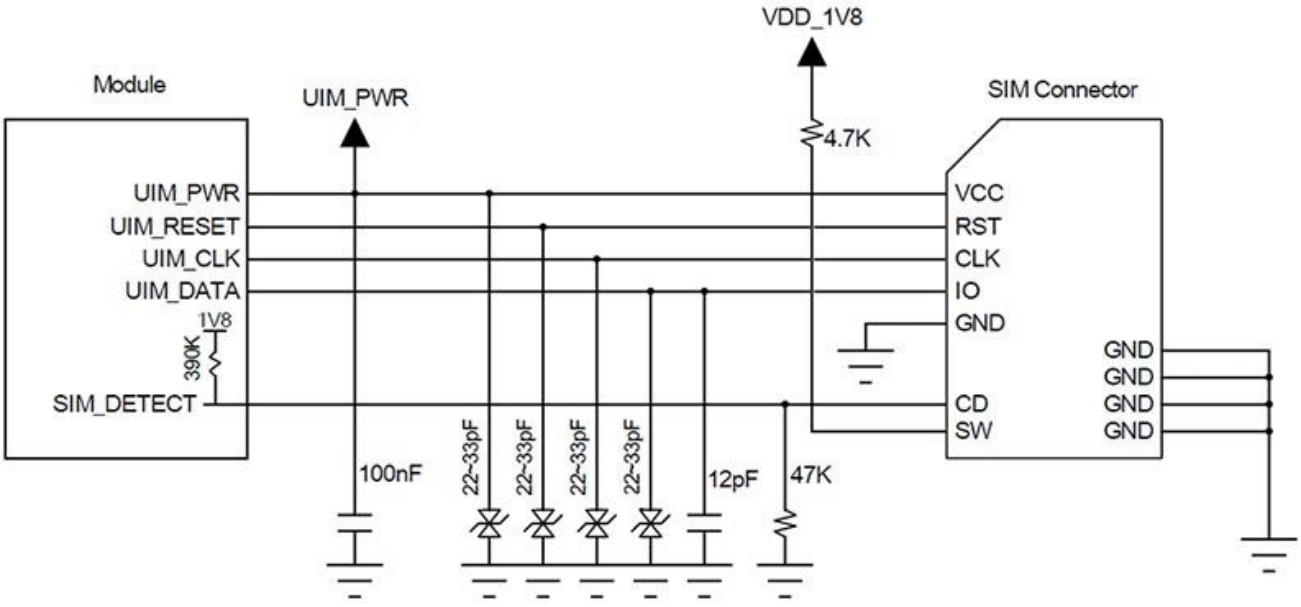


Figure 3-13 Reference circuit for N.O. SIM card slot

The principles of the N.O.SIM card slot are described as follows:

- When the SIM card is removed, CD and SW pins are open-circuited, and the SIM_DETECT pin is at low level.
- When the SIM card is inserted, CD and SW pins are short-circuited, and the SIM_DETECT pin is at high level.

3.5.4. USIM Hot Plug

The AIW-356 DQ-E01 module supports the SIM card hot plug function, and determines whether the SIM card isinserted or removed by detecting the SIM_DETECT pin state of the SIM card slot.

The SIM card hot plug function can be configured by using **AT+MSMPD** command, and the description forAT command is shown in the following table:

AT Command	Hot-plug Detection	Function Description
AT+MSMPD=1	Enable	By default, the SIM card hot plug detection function is enabled. The module can detect whether the SIM card is inserted or not through the SIM_DETECT pin state.
AT+MSMPD=0	Disable	The SIM card hot plug detect function is disabled. The module reads the SIM card when starting up, withoutdetecting the SIM_DETECT status.

Table 3-12 Hot plug AT command

After the SIM card hot plug detection function is enabled, the module detects that the SIM card is inserted when the SIM_DETECT pin is high, then executes the initialization program and finishes the network registration after reading the SIM card information. When the SIM_DETECT pin is low, the module determines that the SIM card is removed and does not read the SIM card.

Note:

By default, SIM_DETECT is active-high, which can be switched to active-low by the AT command.Please refer to the AT Commands Manual for the AT command.

3.5.5. USIM Design Requirements

The SIM card circuit design shall meet the EMC standards and ESD requirements with the improvedcapability to resist interference, to ensure that the SIM card can work stably. The following guidelines should be noted in case of design:

- The SIM card slot placement should be near the module as close as possible, and away from the RF antenna, DC/DC power supply, clock signal lines, and other strong interference sources.
- The SIM card slot with a metal shielding housing can improve the anti-interference ability.
- The route length between the SIM card slot and the module should not exceed 100mm, or it could reduce the signal quality.
- The UIM_CLK and UIM_DATA signal lines should be isolated by GND to avoid crosstalk interference.
- If it is difficult for the layout, the whole SIM signal lines should be wrapped with GND as a group at least.
- The filter capacitors and ESD devices for SIM card signals should be placed near to the SIM card slot, and the equivalent capacitance of the ESD devices should be within 22pF to 33pF.

3.6. Status Indicators

The AIW-356 DQ-E01 module provides two signals to indicate the operating status of the module, and the statusindicator pins are shown in the following table:

Pin	Pin Name	I/O	Reset Value	Pin Description	Type
10	LED1#	O	T	System status LED, open drain output.	-
23	WOWWAN#	O	PD	Module wakes up Host (AP)	1.8V

Table 3-13 Working status indication

3.6.1. LED#1 Signal

The LED#1 signal is used to indicate the operating status of the module, and the detailed description is shown in the following table:

Module Status	LED1# Signal
RF function ON	Low level (LED On)
RF function OFF	High level (LED Off)

Table 3-14 LED working status indication

The LED driver circuit is shown in Figure 3-14:

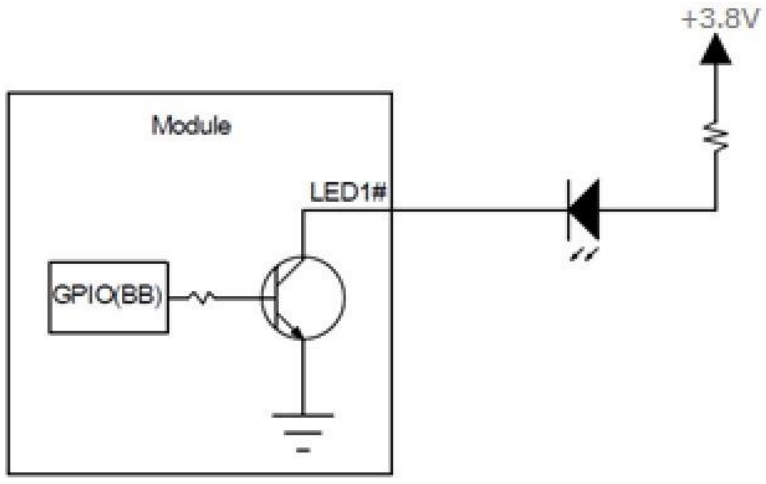


Figure 3-14 LED driver circuit

Note:

Module's internal LED pin driver current < 10mA. The resistance of LED current-limiting resistor is selected according to the driving voltage and the driving current.

3.6.2. WOWWAN# Signal

The WOWWAN# signal is used to wake up the Host (AP) when a data request is received. The definition of WOWWAN# signal is as follows:

Operating Mode	WOWWAN# Signal
Call, SMS or data requests	Pulled down for 1s and then pulled up (pulse signal, configurable by AT command).
Idle/Sleep	High level

Table 3-15 WOWWAN# working status indication

The WOWWAN# timing is shown in Figure 3-21:

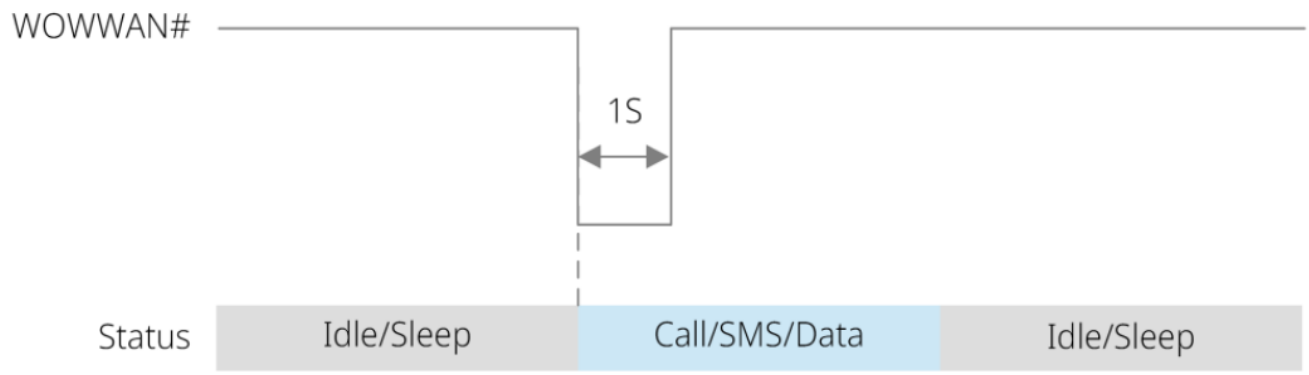


Figure 3-15 WOWWAN# timing

3.7. Interrupt Controls

AIW-356 DQ-E01 module provides 3 interrupt signals, and the pin definition is as follows:

Pin	Pin Name	I/O	Reset Value	Pin Description	Type
8	W_DISABLE1#	I	PU	Disable flight mode of the WWAN module. Active low.	1.8V/3.3V
25	DPR	I	PU	Dynamic power control for SARinterrupt detection, active low. Reserved	1.8V/3.3V
26	W_DISABLE2#	I	PU	Disable GNSS. Active low	1.8V/3.3V

Table 3-16 Interrupt control signal

3.7.1. W_DISABLE

The module provides a hardware pin to enable/disable WWAN RF function. Set **AT+GTFMODE=1** to enable this pin and the function can also be controlled by the AT command. The module enters the Flight mode after the RF function is disabled. The definition of W_DISABLE1# signal is as below table:

W_DISABLE1# Signal	Function
High/Floating	WWAN function is enabled, and the module exits the Flight mode.
Low	WWAN function is disabled, and the module enters Flight mode.

Table 3-17 W_ DISABLE1# signal function definition

The module provides a hardware pin to enable/disable GNSS function, as listed in the following table.

W_DISABLE2# Signal	Function
High/Floating	Enable GNSS
Low	Disable GNSS

Table 3-18 W_ DISABLE2# signal function definition

Note:

The function of W_DISABLE1# can be customized, please refer to the software description.

3.7.2. BODYSAR

AIW-356 DQ-E01 module supports Body SAR function by detecting the DPR pin. The voltage level of DPR is high by default. When the AP detects closing body through SAR sensor (distance sensor), the AP pulls down the DPR signal. In this case, the module lowers down its transmitting power to its preset threshold value, thus reducing the RF radiation on the human body. The threshold of transmitting power can be set by the AT Commands or DPR tool. The definition of DPR signal is shown in the following table:

DPR Signal	Function
High/Floating	The module keeps the default transmitting power.
Low	Lower the maximum transmitting power value of the module-reserved.

Table 3-19 DPR signal function definition

3.8. Antenna Tuner Interfaces

The module supports ANT Tuner interfaces with two different control modes, i.e. MIPI interface and 3bit GPO interface. Through using the antenna tuber interface and external antenna tuner switch, the module can be flexibly configured with the bands of antenna to improve the antenna's working efficiency and save space for the antenna.

Pin	Pin Name	I/O	Reset Value	Pin Description	Type
56	RFFE_SCLK	O	PD	MIPI Interface clock signal, for antenna tuner to use	1.8V
58	RFFE_SDATA	I/O	PD	MIPI Interface data signal, for antenna tuner to use	1.8V
61	ANTCTL1	O	PD	Antenna matching and adjustment, Bit1	1.8V
63	ANTCTL2	O	PD	Antenna matching and adjustment, Bit2	1.8V
65	ANTCTL3	O	PD	Antenna matching and adjustment, Bit3	1.8V

Table 3-20 Definition of antenna tuner interface

3.9. M.2 Interface Type

The AIW-356 DQ-E01 module provides 4 configuration pins, they are output pins, and used to read the high/low level for the host system and detect the type of the module inserted into the host system M.2 slot. If the host system does not need to detect the module type and function, these 4 pins can be left floating. This module is configured as the WWAN-USB3.1 type M.2 module:

Pin	Pin Name	I/O	Reset Value	Pin Description	Type
1	CONFIG_3	O	-	NC	-
21	CONFIG_0	O	-	NC	-
69	CONFIG_1	O	L	Internally connected to GND	-
75	CONFIG_2	O	-	NC	-

Table 3-21 Configuration interface

4 RF

4.1. RF Interface

4.1.1. RF Interface Functionality

AIW-356 DQ-E01 module supports four RF connectors used for external antenna connection. As shown in Figure 4-1

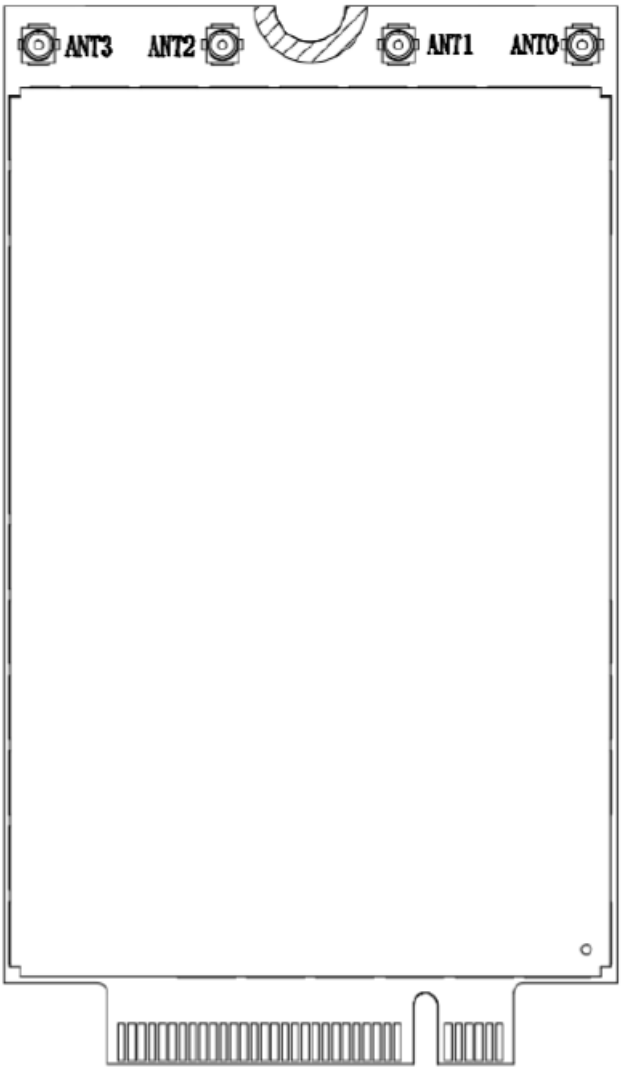


Figure 4-1 RF connectors

4.1.2. Antenna Performance Requirement

Antenna Performance Requirement	
Input impedance:	50 Ω
Input power:	>28dBm
VSW:	<2:1
Antenna gain:	<3.6dBi
Isolation between antennas:	>25dB
Antenna wire insertion loss:	LB (< 1 GHz) < 0.3 dB/MB (1 ~ 2.7 GHz) < 0.8 dB/HB (> 2.7 GHz) < 1.2 dB

Table 4-1 RF connector performance

4.1.3. RF Connector Performance

Rated Condition		Environment Condition
Frequency Range	DC to 6GHz	Temperature Range
Characteristic Impedance	50Ω	–40°C to +85°C

Table 4-2 RF connector performance

4.1.4. RF Connector Dimensions

AIW-356 DQ-E01 module adopts standard M.2 module RF connectors, the model name is 818004607 from ECT Corporation, and the connector size is 2mm × 2mm × 0.6mml, as shown in the following figure:

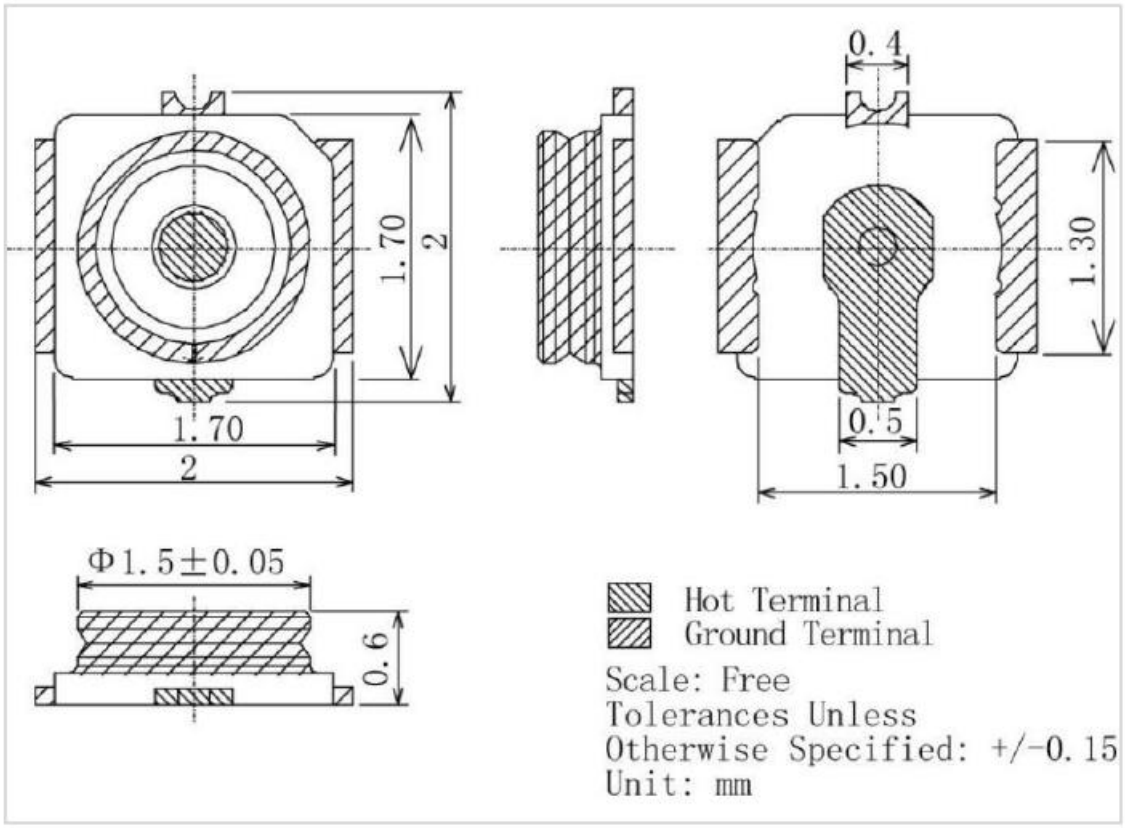


Figure 4-2 RF connector dimensions

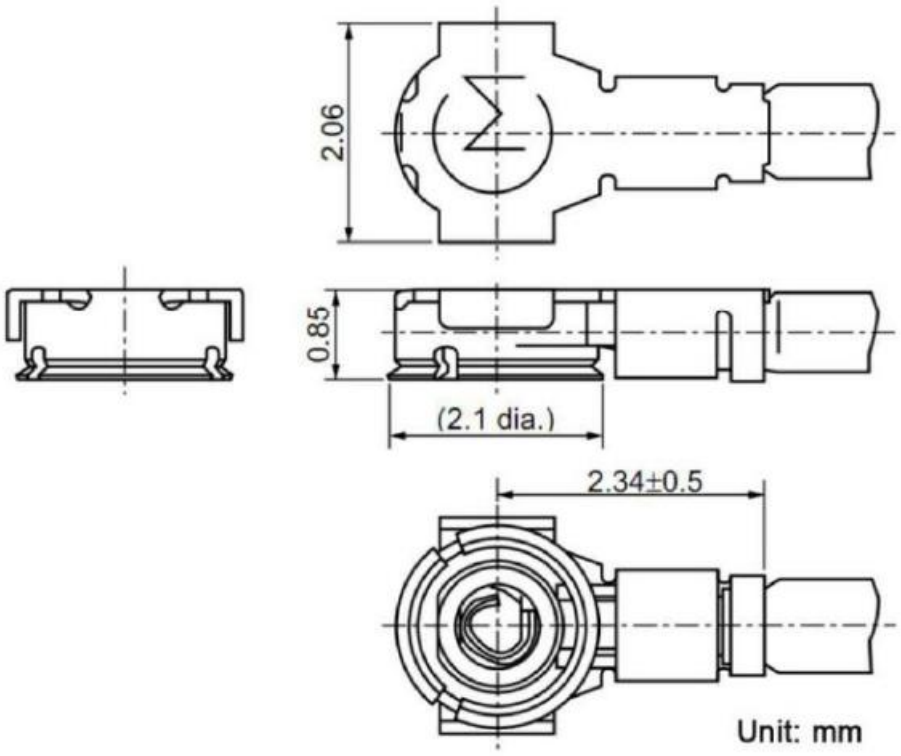


Figure 4-3 0.81mm coaxial cable matched RF connector dimensions

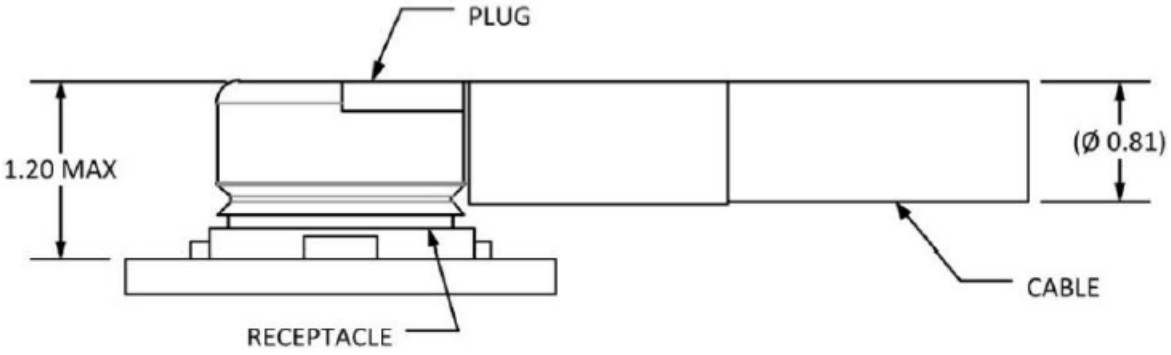


Figure 4-4 Schematic diagram of 0.81mm coaxial cable antenna connected to the RF connector

4.1.5. RF Connector Assembly

Keep RF connector parallel with the main board, and then press the RF connector into the RF connector base.

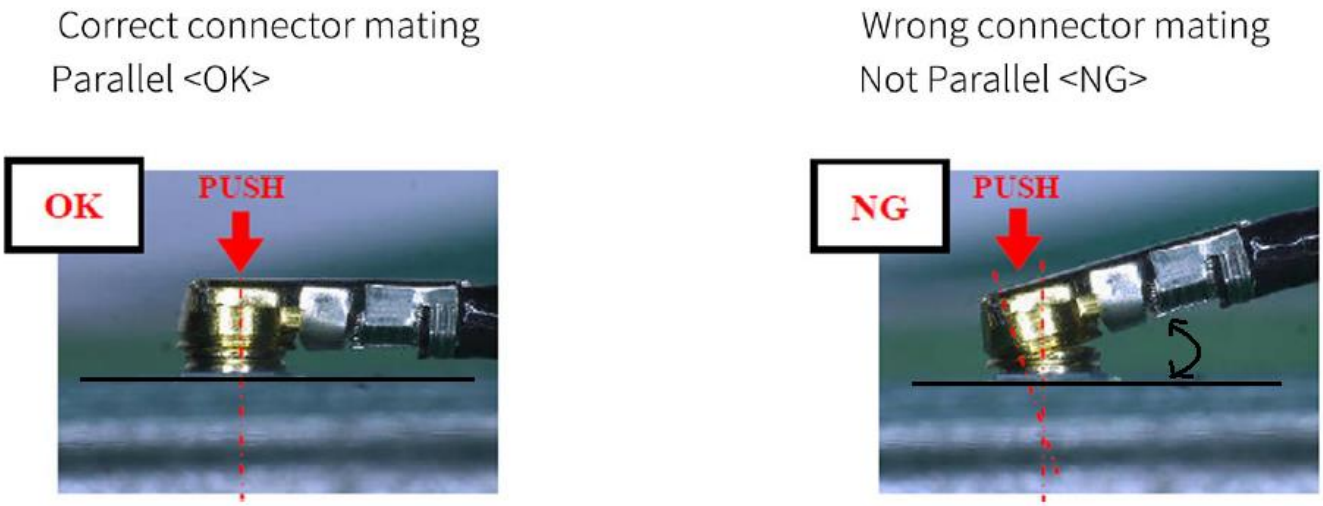


Figure 4-5 RF connector installation method

4.2. Operating Band

The antenna operating bands of the AIW-356 DQ-E01 module are as follows:

Operating Band	Frequency	Mode	Tx (MHz)	Rx (MHz)
Band 1	2100MHz	LTE FDD	1920–1980	2110–2170
Band 3	1800MHz	TE FDD	1710–1785	1805–1880
Band 5	850MHz	LTE FDD	824–849	869–894
Band 7	2600Mhz	TE FDD	2500–2570	2620–2690
Band 8	900MHz	TE FDD	880–915	925–960
Band 18	850MHz	TE FDD	815–830	860–875
Band 19	850MHz	TE FDD	830–845	875–890
Band 26	850MHz	TE FDD	814–849	859–894
Band 28	700MHz	TE FDD	703–748	758–803
Band 39	1900MHZ	LTE TDD	1880–1920	1880–1920
Band 41	2500MHZ	LTE TDD	2496–2690	2496–2690
Band 42	3500MHZ	LTE TDD	3400-3600	3400-3600
n1	2100MHz	NR	1920–1980	2110–2170
n3	1800MHz	NR	1710–1785	1805–1800
n7	2600MHz	NR	2500–2570	2620–2690
n8	900MHz	NR	880–915	925–960
n28	700MHz	NR	703–748	758–803
n41	2500MHZ	NR	2496–2690	2496–2690
n77	3700MHZ	NR	3300-4200	3300-4200
n78	3500MHZ	NR	3300-3800	3300-3800

Operating Band	Frequency	Mode	Tx (MHz)	Rx (MHz)
n79	4700MHZ	NR	4400-5000	4400-5000
GPS L1	-	-	-	1575.42±1.023
GLONASS L1	-	-	-	1602.5625±4
BDS	-	-	-	1561.098±2.046
Galileo	-	-	-	1559-1592
QZSS	-	-	-	1575.42±1.023

Table 4-2 Operating frequency bands

4.3. Transmitting Power

The transmitting power for each band of the AIW-356 DQ-E01 module is shown in the following table:

Mode	Band	3GPP Requirement	Max Power	Unit
LTE	Band 1	23±2.7	23±1.5	dBm
	Band 3	23±2.7	23±1.5	dBm
	Band 5	23±2.7	23±1.5	dBm
	Band 7	23±2.7	23±1.5	dBm
	Band 8	23±2.7	23±1.5	dBm
	Band 18	23±2.7	23±1.5	dBm
	Band 19	23±2.7	23±1.5	dBm
	Band 26	23±2.7	23±1.5	dBm
	Band 28	23+2.7/-3.2	23±1.5	dBm
	Band 39	23±2.7	23±1.5	dBm
	Band 41	23±2.7	23±1.5	dBm
	Band 42	23+3/-4	23±1.5	dBm

Mode	Band	3GPP Requirement	Max Power	Unit
5G NR	n1	23±2±TT	23±1.5	dBm
	n3	23±2±TT	23±1.5	dBm
	n7	23±2±TT	23±1.5	dBm
	n8	23±2±TT	23±1.5	dBm
	n28	23+2/-2.5	23±1.5	dBm
	n41	23±2±TT	23±1.5	dBm
	n41 UL MIMO	24.5+2+TT/-3-TT	21.5±1.5	dBm
	n77	23+2+TT/-3-TT	23±1.5	dBm
	n77 UL MIMO	24.5+2+TT/-3-TT	21.5±1.5	dBm
	n78	23+2+TT/-3-TT	23±1.5	dBm
	n78 HPUE	26+2+TT/-3-TT	26±1.5	dBm
	n78 UL MIMO	24.5+2+TT/-3-TT	24.5±1.5	dBm
	n79	23+2+TT/-3-TT	23±1.5	dBm
	n79 UL MIMO	24.5+2+TT/-3-TT	21.5±1.5	dBm

Table 4-3 Transmitting power for each band

Note:

1. LTE Max Power is measured in UL 10MHz 1RB.
2. 5G NR Max Power is measured in UL FDD 10MHz, TDD 100MHz (N38 20 MHz)DFT-s-OFDM/QPSK Inner Full RB.
3. 5GNR UL MIMO Max Power is measured in TDD 100MHz CP-OFDM/QPSK Inner Full RB.
4. TT: Test Tolerance.

4.4. Receiving Sensitivity

4.4.1. Dual-Antenna Receiving Sensitivity

The following table lists dual-antenna sensitivity of the AIW-356 DQ-E01 module on each band:

Mode	Band	3GPP Requirement	Rx Sensitivity (Typical)	Unit
WCDMA	Band 1	-106.7	-112.6	dBm
	Band 3	-104.7	-115.7	dBm
	Band 5	-103.7	-115.3	dBm
LTE FDD (10MHz)	Band 1	-96.3	-98.6	dBm
	Band 3	-93.3	-99.9	dBm
	Band 5	-94.3	-102	dBm
	Band 7	-94.3	-100.4	dBm
	Band 8	-93.3	-102.4	dBm
	Band 20	-93.3	-102.8	dBm
	Band 28	-94.8	-103	dBm
	Band 32	-96.3	-99.3	dBm
	Band 66	-95.8	-99.5	dBm
LTE TDD (10MHz)	Band 38	-94.3	-99.9	dBm
	Band 40	-96.3	-98.7	dBm
	Band 41	-94.3	-99.5	dBm
	Band 42	-95.0	-100.8	dBm
	Band 43	-95.0	-100.7	dBm

Mode	Band	3GPP Requirement	Rx Sensitivity (Typical)	Unit
NR FDD (10MHz)	n1	-96.8	-100.1	dBm
	n3	-93.8	-100.4	dBm
	n5	-94.8	-101.3	dBm
	n7	-94.8	-100	dBm
	n8	-93.8	-101.5	dBm
	n20	-93.8	-101.5	dBm
	n28	-95.5	-103.2	dBm
	n66	-96.3	-99.6	dBm
NR TDD (100 MHz)	n38	-90.7	-94.3	dBm
	n40	-87.6	-90.8	dBm
	n41	–84.7	-89.5	dBm
	n75	–96.8	-101.2	dBm
	n77	–85.1	-89.6	dBm
	n78	–85.6	-89.4	dBm

Table 4-4 Dual-antenna sensitivity on each frequency band

Note:

1. LTE receiving sensitivity is measured in DL 10MHz full RB.
2. 5GNR FDD receiving sensitivity is measured in DL 10MHz SCS=15KHz Full RB.
3. 5GNR TDD receiving sensitivity is measured in DL 100MHz SCS=30KHz Full RB.

4.4.2. Four-Antenna Receiving Sensitivity

AIW-356 DQ-E01 module supports four antennas on some middle/high bands, and the receiver sensitivity of the AIW-356 DQ-E01 module on these middle/high bands is shown in below table:

Mode	Band	3GPP Requirement	Rx Sensitivity Typical	Unit
LTE FDD (10MHz)	Band 1	-99.0	-103.6	dBm
	Band 3	-96.0	-103.8	dBm
	Band 5	-97.0	-105.7	dBm
	Band 7	-97.0	-103.3	dBm
	Band 20	-96.0	-105.3	dBm
	Band 28	-97.5	-105.8	dBm
	Band 32	-99.0	-102.5	dBm
	Band 66	-98.5	-103.5	dBm
LTE TDD (10MHz)	Band 38	-97.0	-102.5	dBm
	Band 40	-99.0	-102.1	dBm
	Band 41	-97.0	-102.9	dBm
	Band 42	-97.2	-103.1	dBm
	Band 43	-97.2	-103.6	dBm

Mode	Band	3GPP Requirement	Rx Sensitivity Typical	Unit
NR FDD (10MHz)	n1	–99.5	-103.8	dBm
	n3	–96.5	-103.7	dBm
	n5	–97.5	-104.5	dBm
	n7	–97.5	-103.5	dBm
	n20	–96.5	-104.5	dBm
	n28	–98.2	-105.1	dBm
	n66	–99.0	-103.5	dBm
NR TDD (10MHz)	n38(40 MHz)	–93.4	-97.8	dBm
	n40(40 MHz)	–90.3	-93.8	dBm
	n41	–87.4	-92.5	dBm
	n77	–87.3	-92.2	dBm
	n78	–87.8	-93	dBm

Table 4-5 Sensitivity of four antenna receiver

Note:

The above values are measured in four antennas condition (ANT0+ ANT1+ ANT2+ ANT3). If only dual antennas are used, the sensitivity of the module will drop about 3dB on each bandof LTE/NR.

4.5. GNSS

AIW-356 DQ-E01 module supports GNSS functions, and adopts RF Diversity and GNSS integrated antenna. GNSS supports GPS/GLONASS/BDS/GALILEO/QZSS. GNSS performance parameters are listed in the following table.

Parameter	Description	Result	Unit
Sensitivity	Acquisition	–148	dBm
	Tracking	–158	dBm
TTFF	Cold Start	40	s
	Warm Start	35	s
	Hot Start	2.5	s
Static Accuracy	Nominal accuracy	2	m

Table 4-6 Performance parameters of GNSS

Note:

The data above is an average value tested on some samples at 25°C temperature.

5 Electrostatic Protection

The module is ESD sensitive component, and the ability to resist static electricity is weak. So ESD precautions that apply to ESD sensitive components should be strictly followed. Proper ESD procedures must be applied throughout the processing, delivery, assembly and operation.

The ESD characteristics are shown in the following table: (Temperature: 25°C, Relative Humidity: 40%).

Test Point	Contact Discharge	Air Discharge
GND	±8 kV	±15 kV
Antenna Interface	±8 kV	NA
Golden Finger	±1 kV	NA

Table 5-1 ESD performance

Note:

ESD performance is the test result of the EVB-M2 evaluation board.

6 Structure Specifications

6.1. Product Appearance

6.2. Structural Dimensions

The structural dimensions of the AIW-356 DQ-E01 module are shown in Figure 6-2:

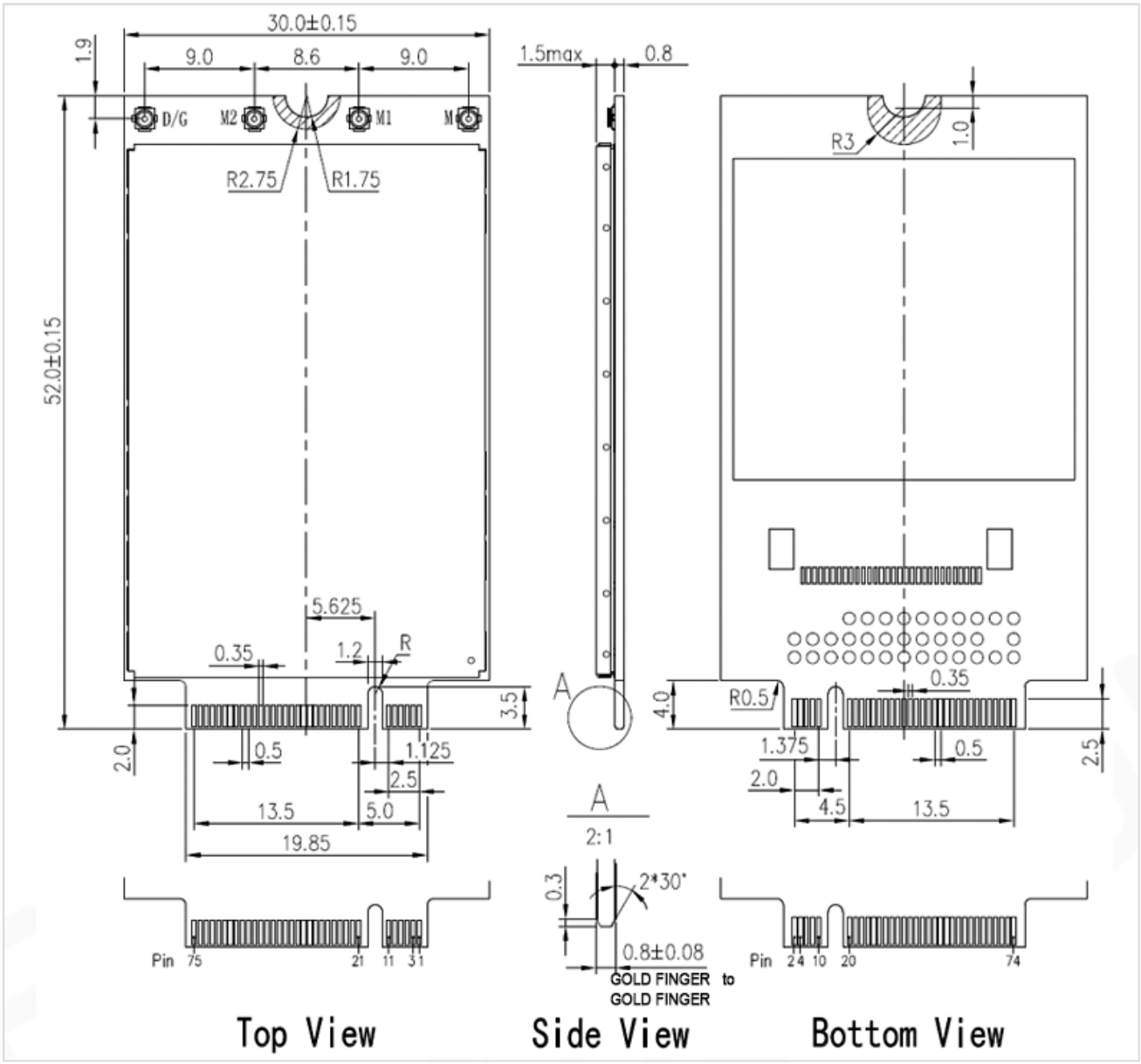


Figure 6-2 Structural dimensions

6.3. M.2 Interface Model

The AIW-356 DQ-E01 M.2 module adopts 75-pin gold finger as external interface, where 67 pins are signal pins and 8 pins are notch pins as shown in Figure 3-1. Based on the M.2 interface definition, AIW-356 DQ-E01 module adopts Type 3052-S3-B interface (30mm × 52mm, maximum component thickness on the top is 1.5mm, PCB thickness is 0.8mm, and KEY ID is B).

6.4. M.2 Connector

The AIW-356 DQ-E01 module connects to AP via M.2 connector. It is recommended to use M.2 connector from LOTES Corporation with the model APCI0026-P001A as shown in Figure 6-2. For the package of connector, please refer to the specification.

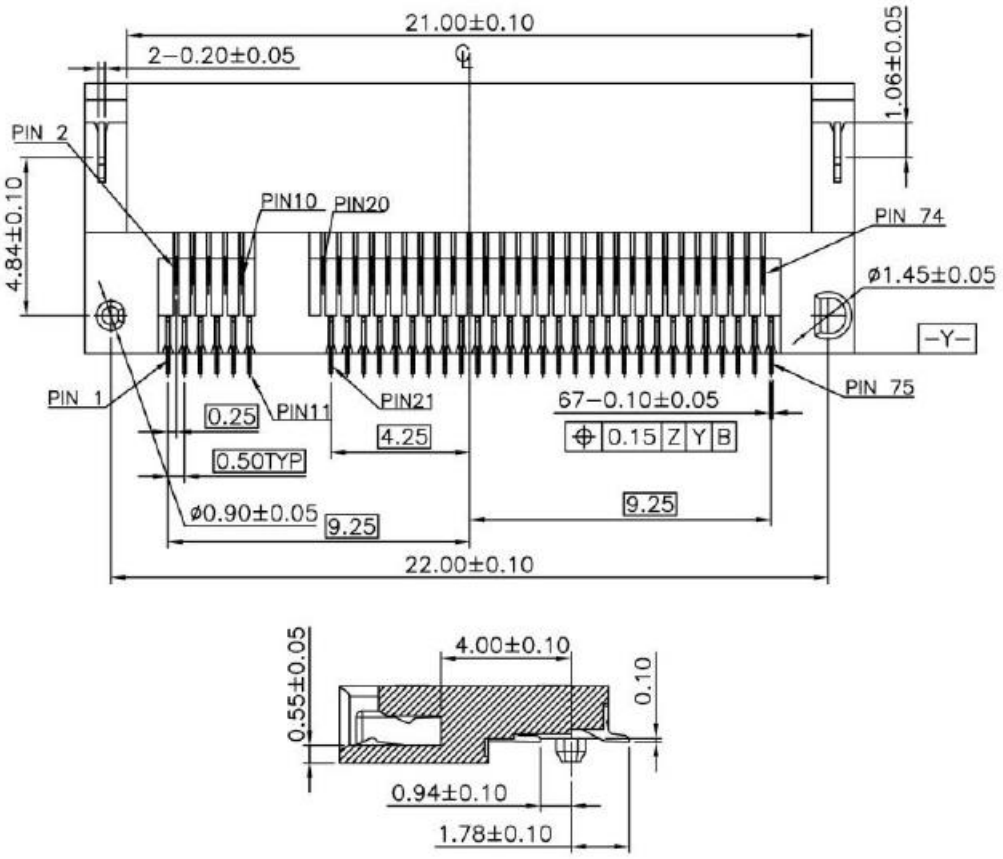


Figure 6-3 M.2 connector dimensions

6.5. Storage life

Storage Conditions (recommended): Temperature is 23±5ºC, relative humidity less than RH 60%. Storage period: Under the recommended storage conditions, the storage life is 12 months.